McSee: Evaluating Advanced Rowhammer Attacks and Defenses via Automated DRAM Traffic Analysis

Patrick Jattke Michele Marazzi Flavien Solt

Max Wipfli Stefan Gloor Kaveh Razavi

COMSEC

ETH zürich

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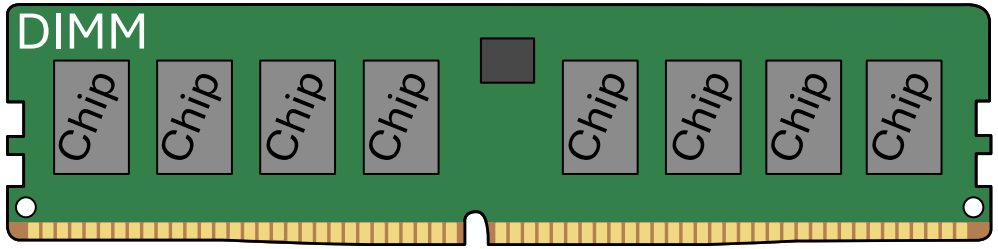
34TH USENIX SECURITY SYMPOSIUM

August 13–15, 2025
Seattle, WA, USA

Track – Hardware Security 3:
Side-Channel and Fault Injection Attacks

A Primer on DRAM and Rowhammer

DIMM Organization



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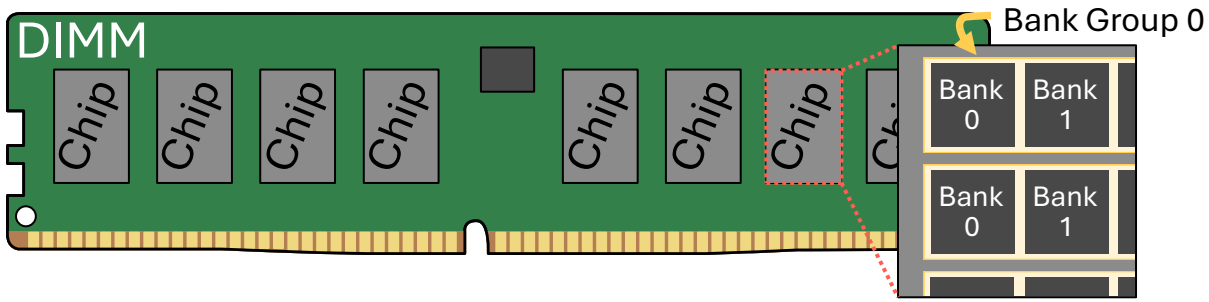

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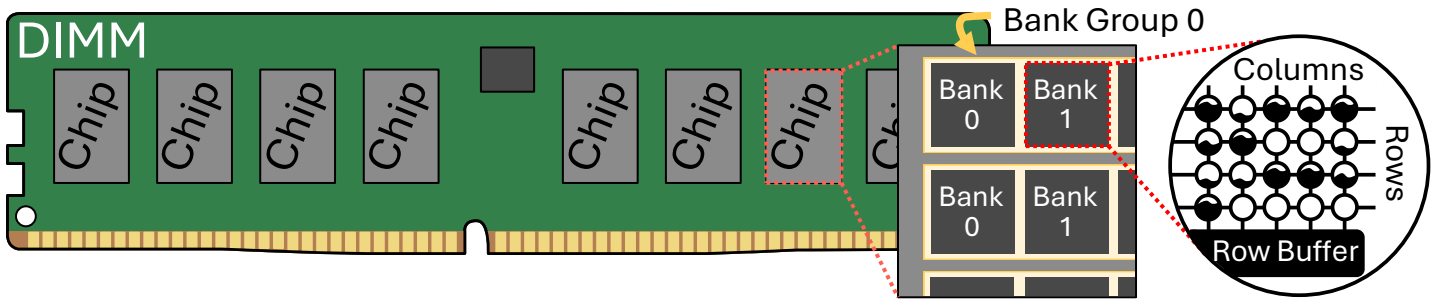

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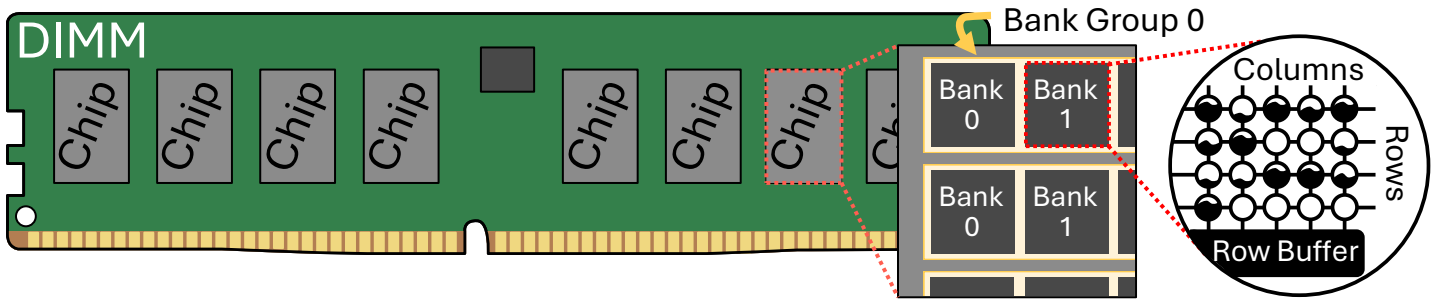
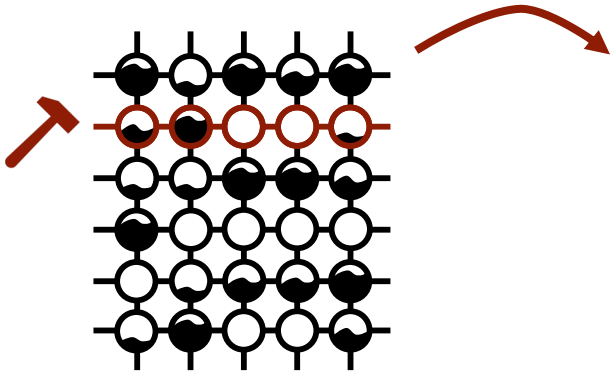


Rowhammer



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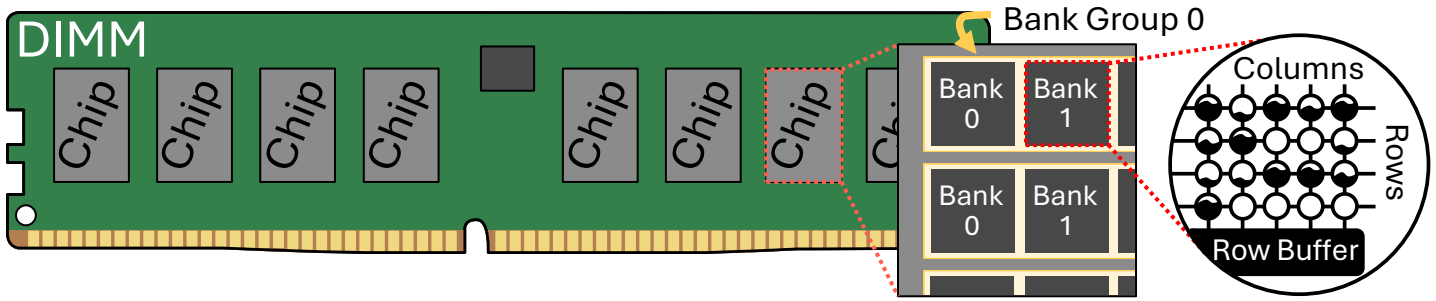
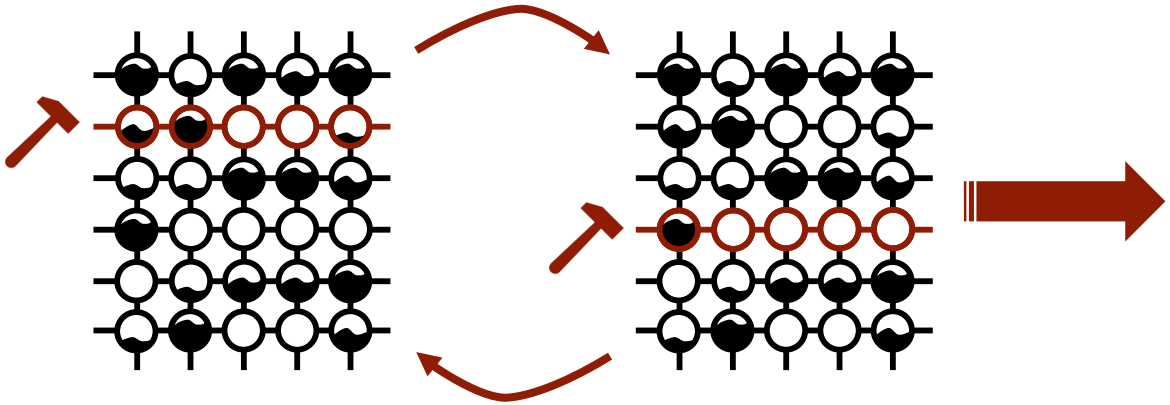


Rowhammer



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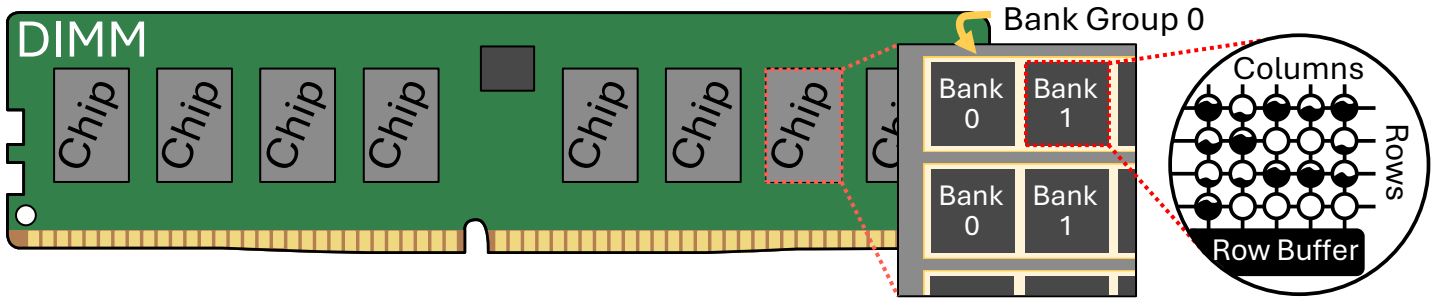

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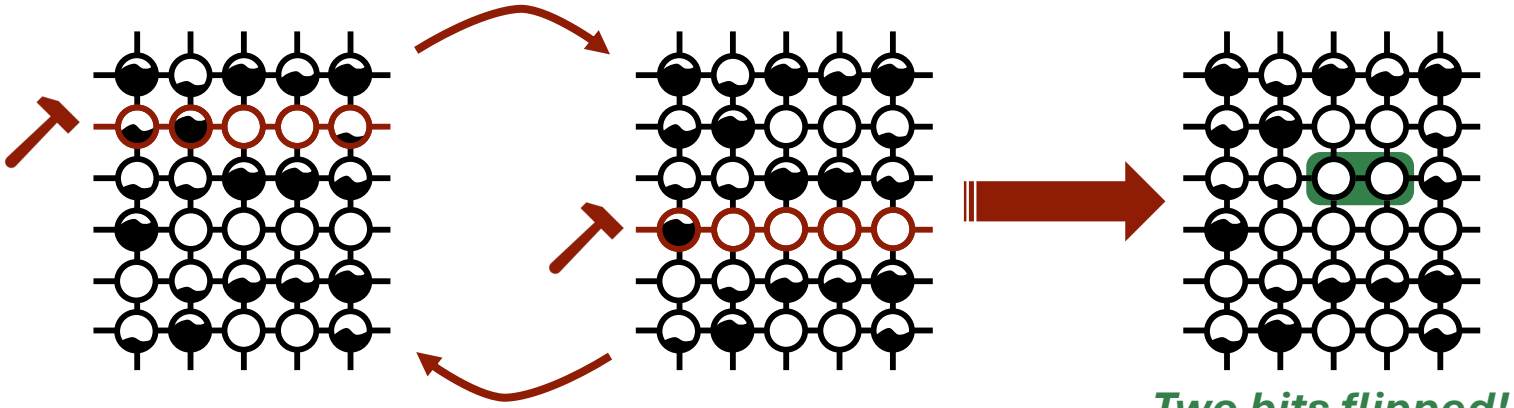

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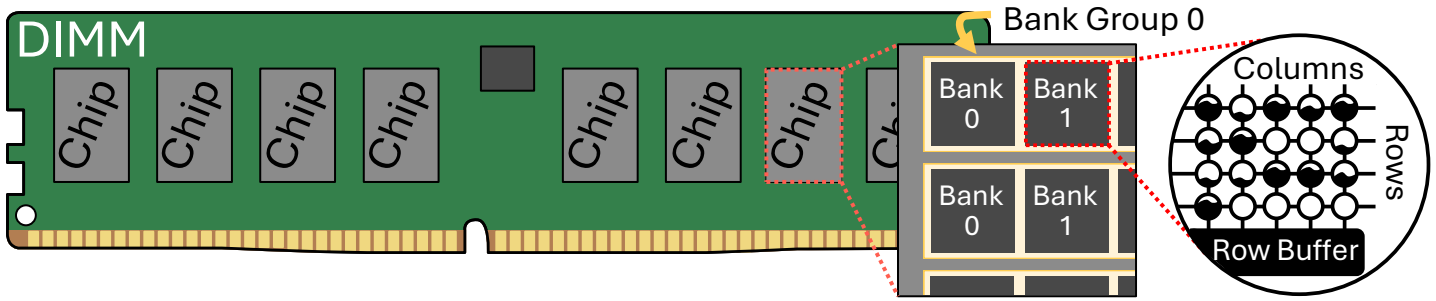

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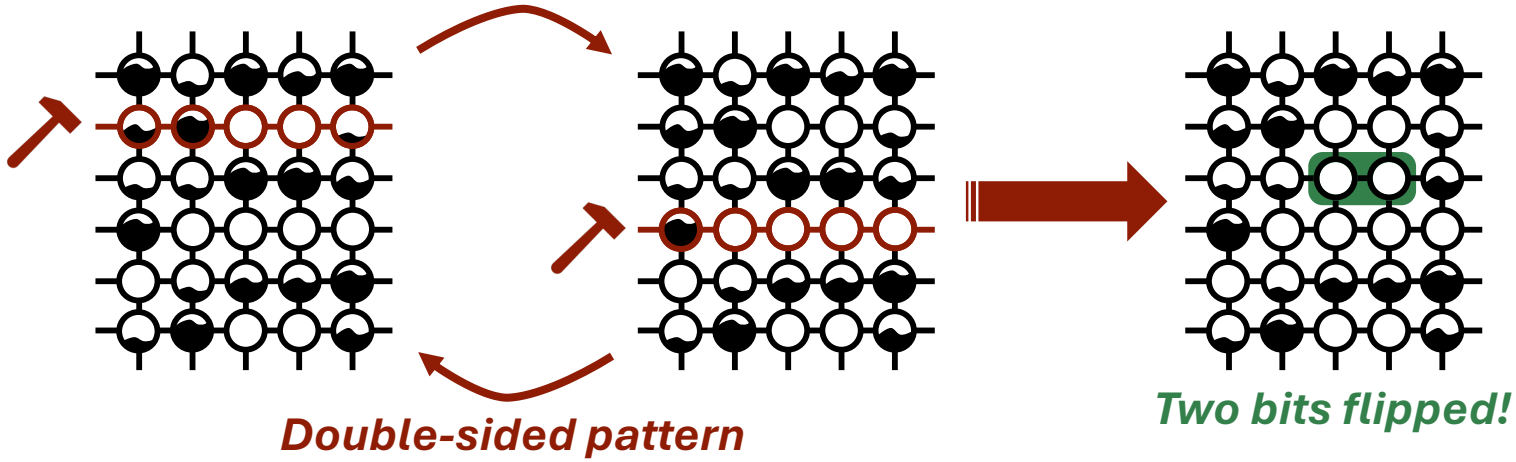
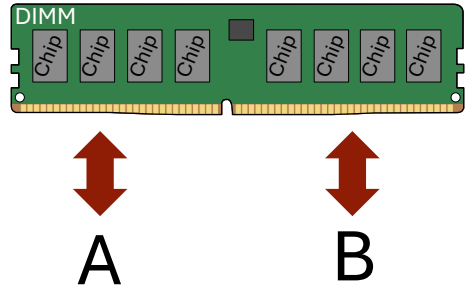


DDR5 Changes



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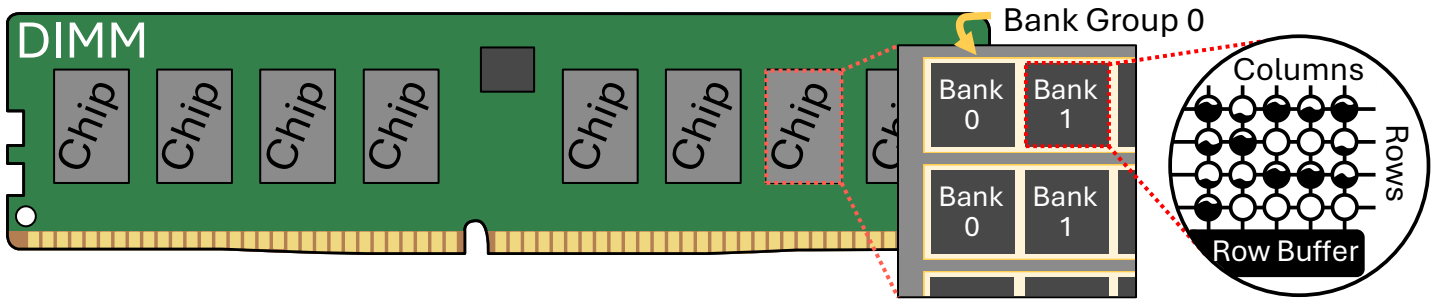
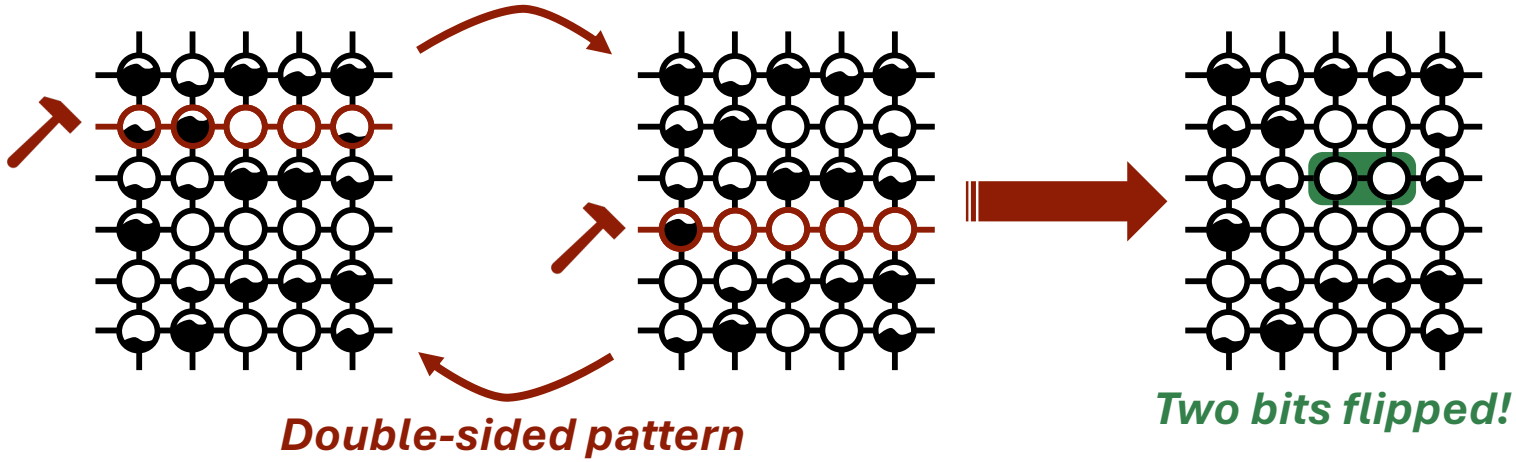


Rowhammer



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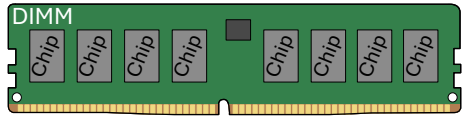
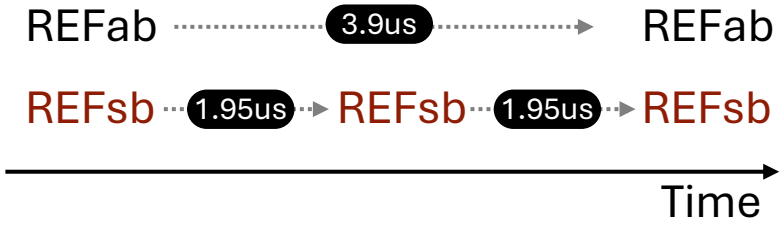


2 Sub-channels

A B

Fine Granularity Refresh



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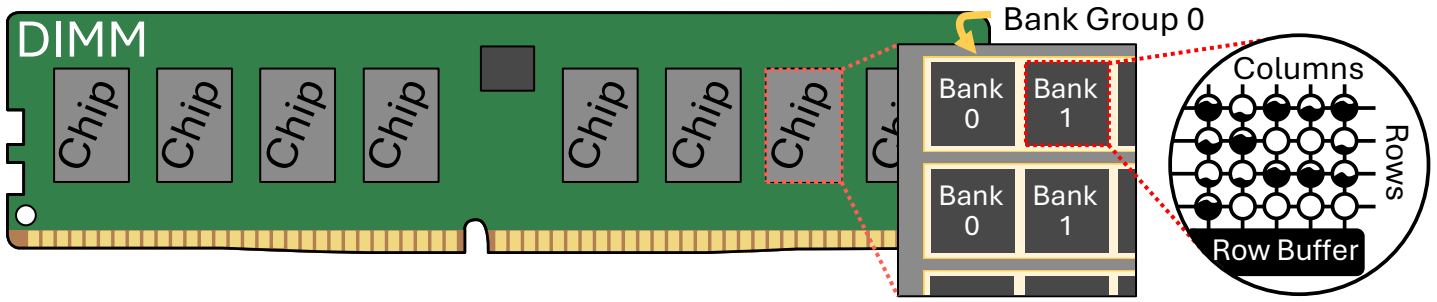
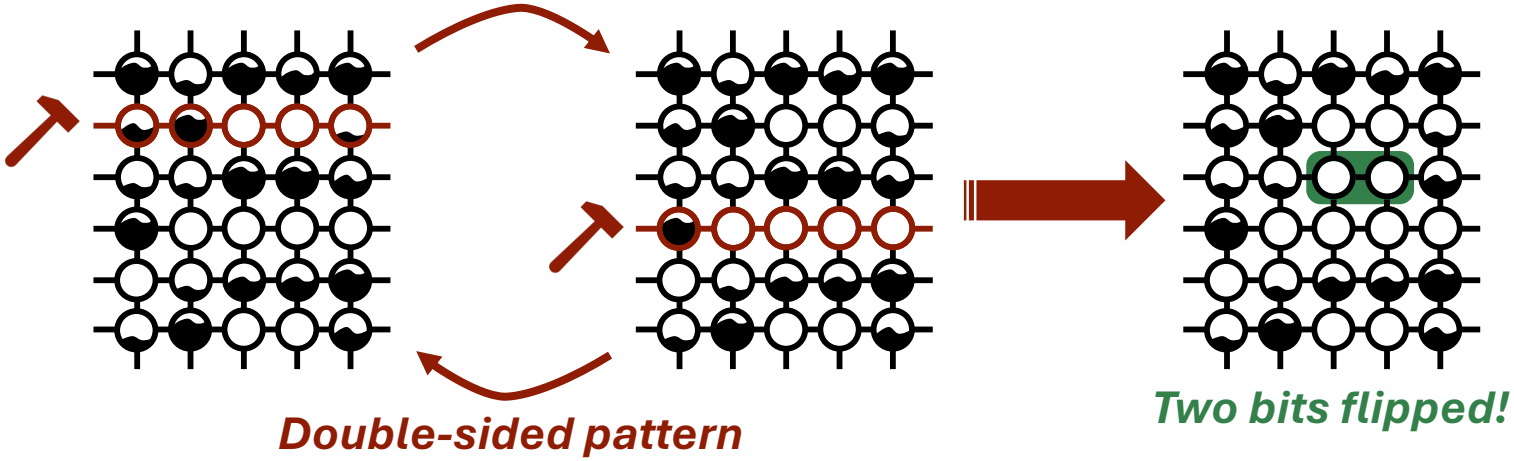


Rowhammer



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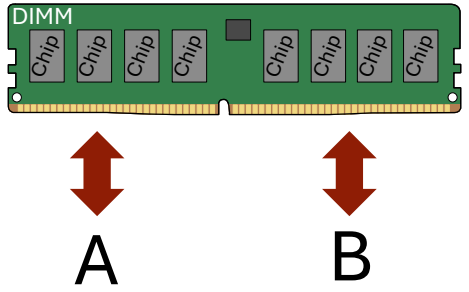

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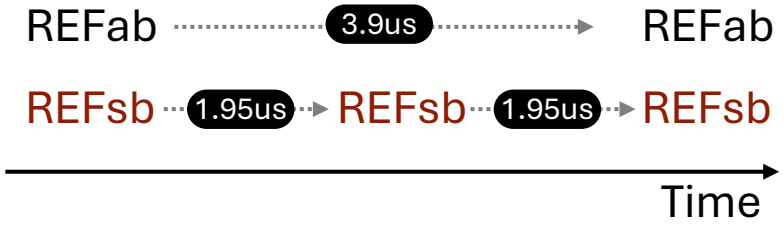
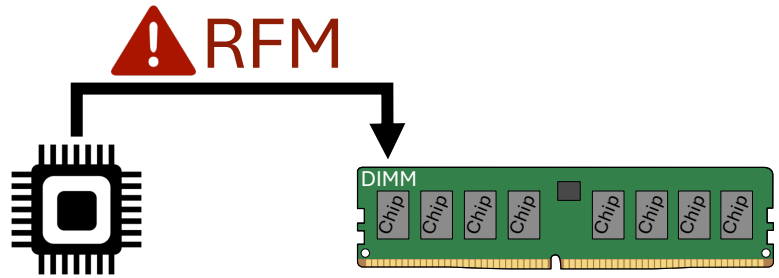
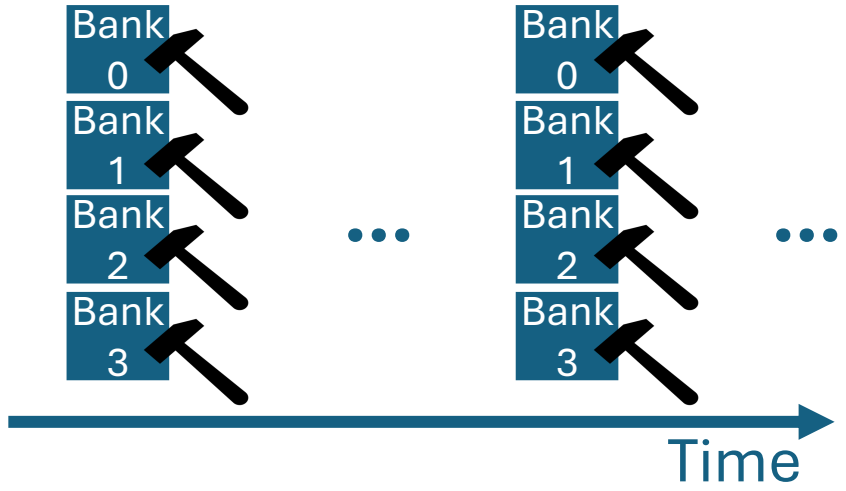


Refresh Management



Rowhammer: An Arms Race in the Dark
Attacks

- Sledgehammer hammers **multiple banks** in parallel.
- More bitflips → easier attacks



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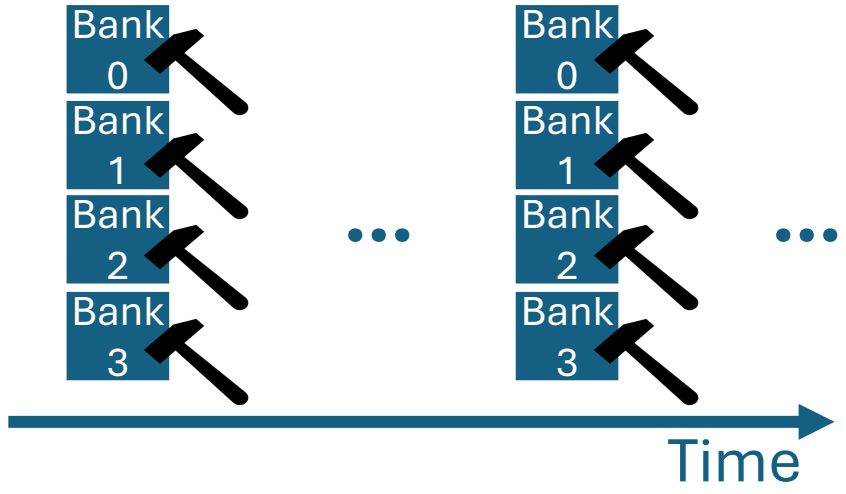
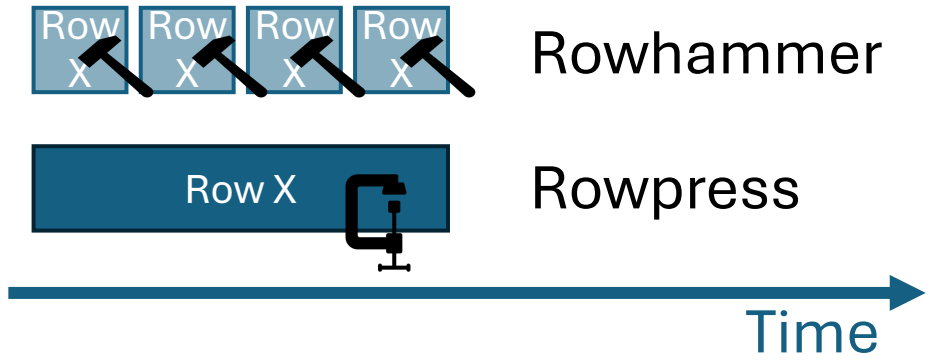


- Rowpress is a new memory disturbance effect.
- Instead of hammering, Rowpress keeps **rows open** for longer.



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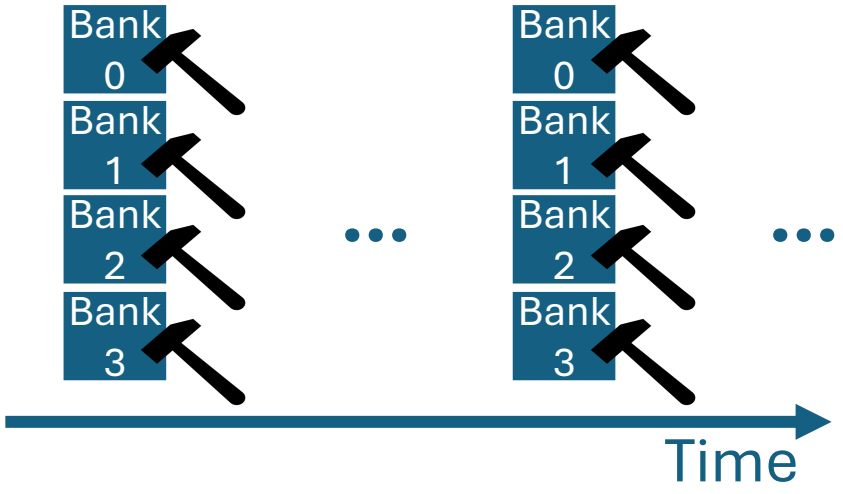

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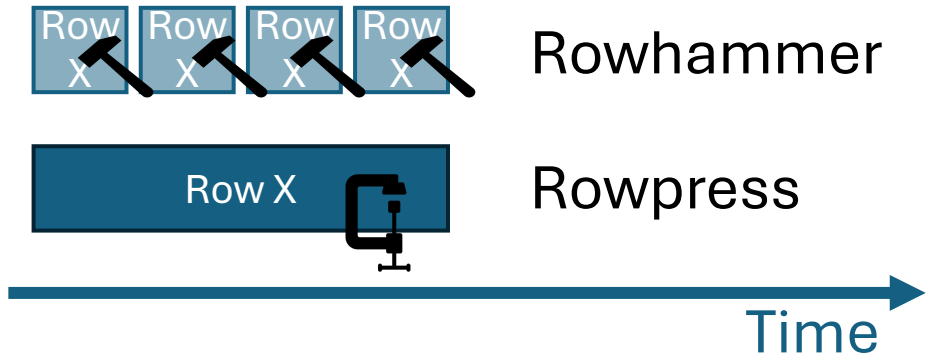

Are advanced attacks exploiting the DRAM device as intended?

Rowhammer: An Arms Race in the Dark
Defenses

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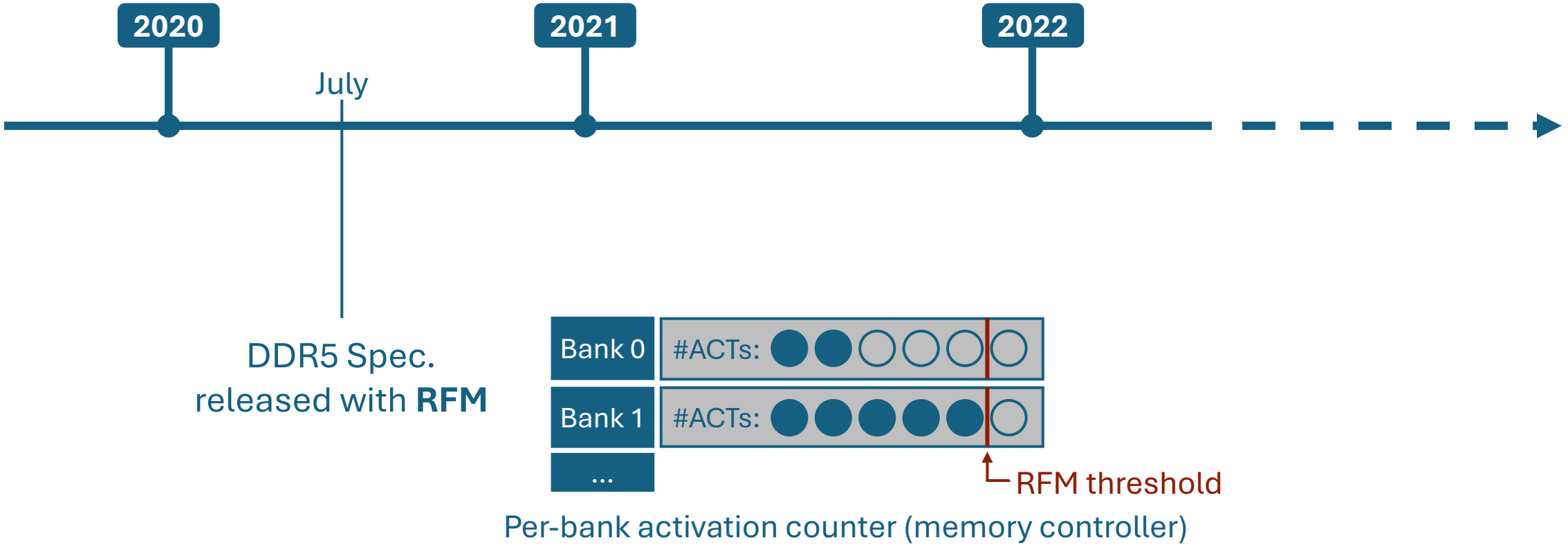
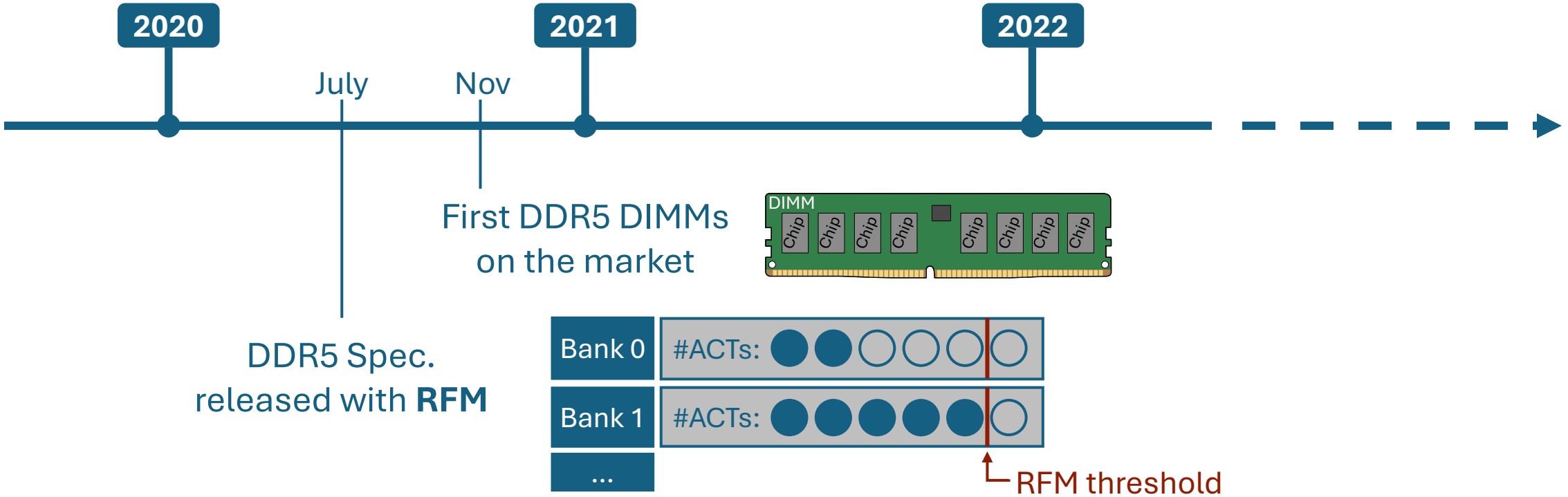
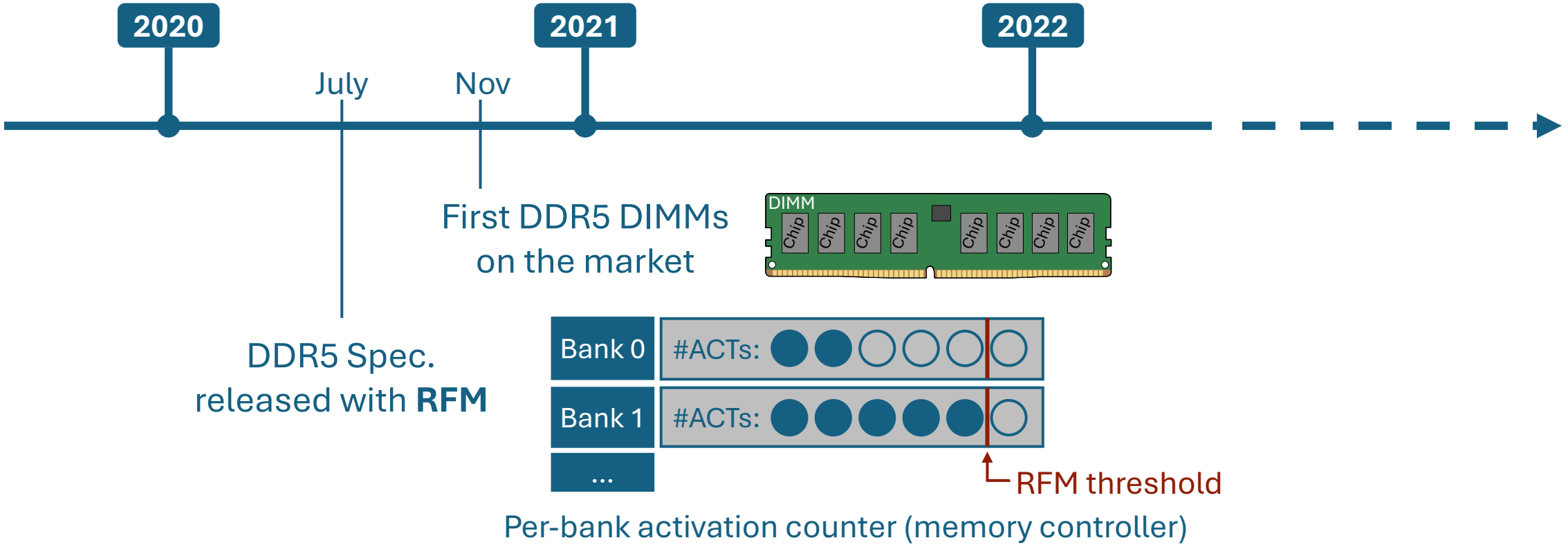
Defenses



Rowhammer: An Arms Race in the Dark
Defenses

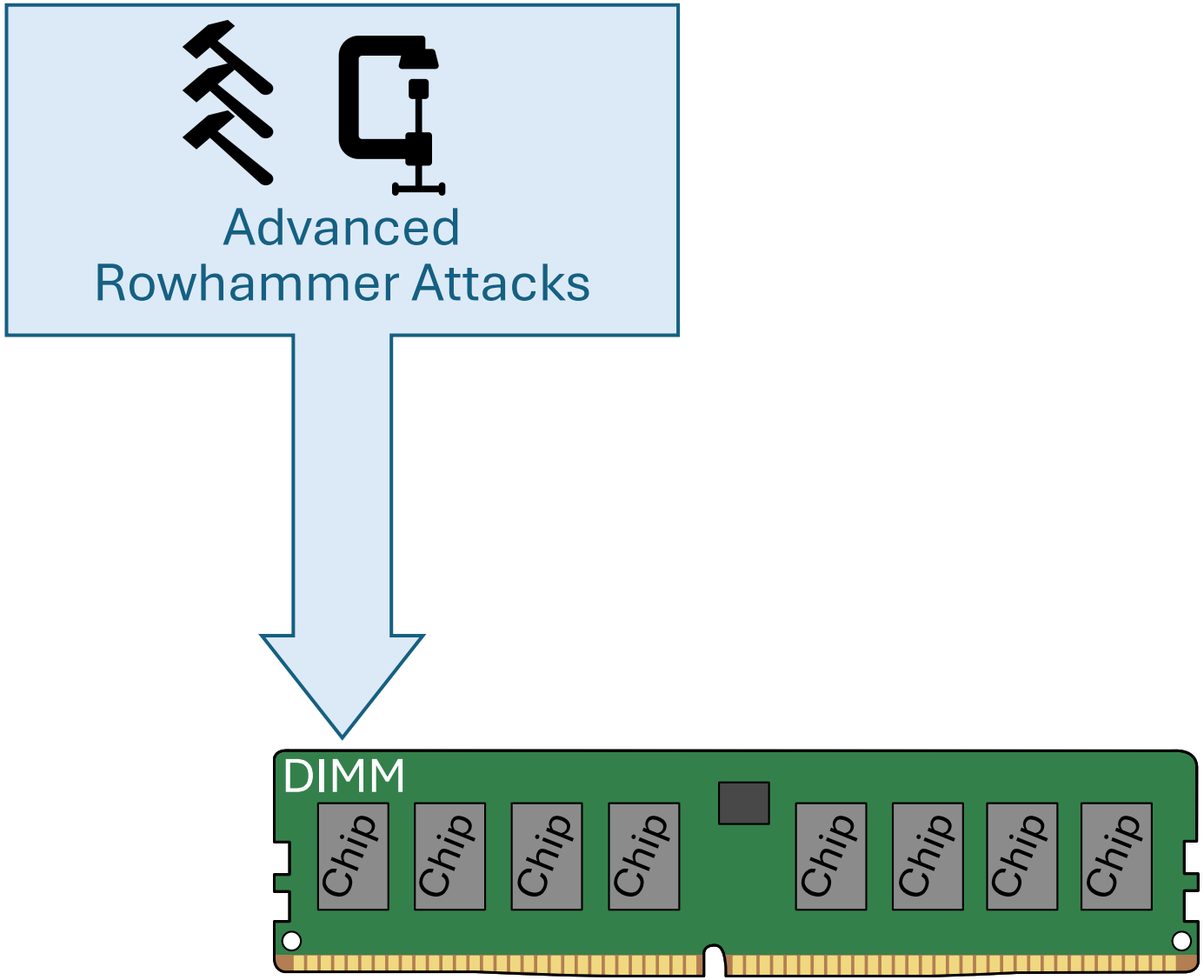


Rowhammer: An Arms Race in the Dark
Defenses

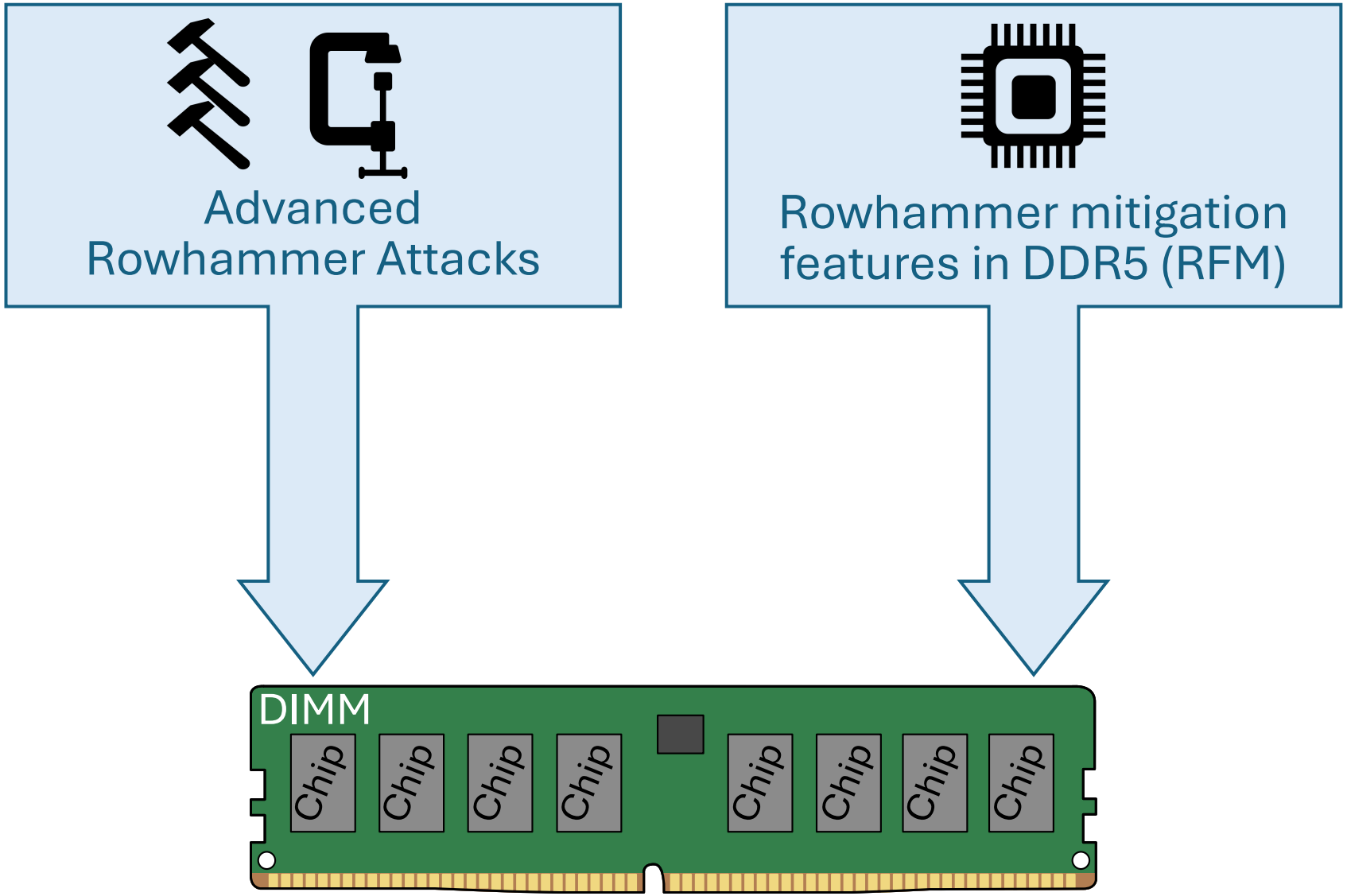


Are CPUs using *optional* DDR5 features to protect against Rowhammer?

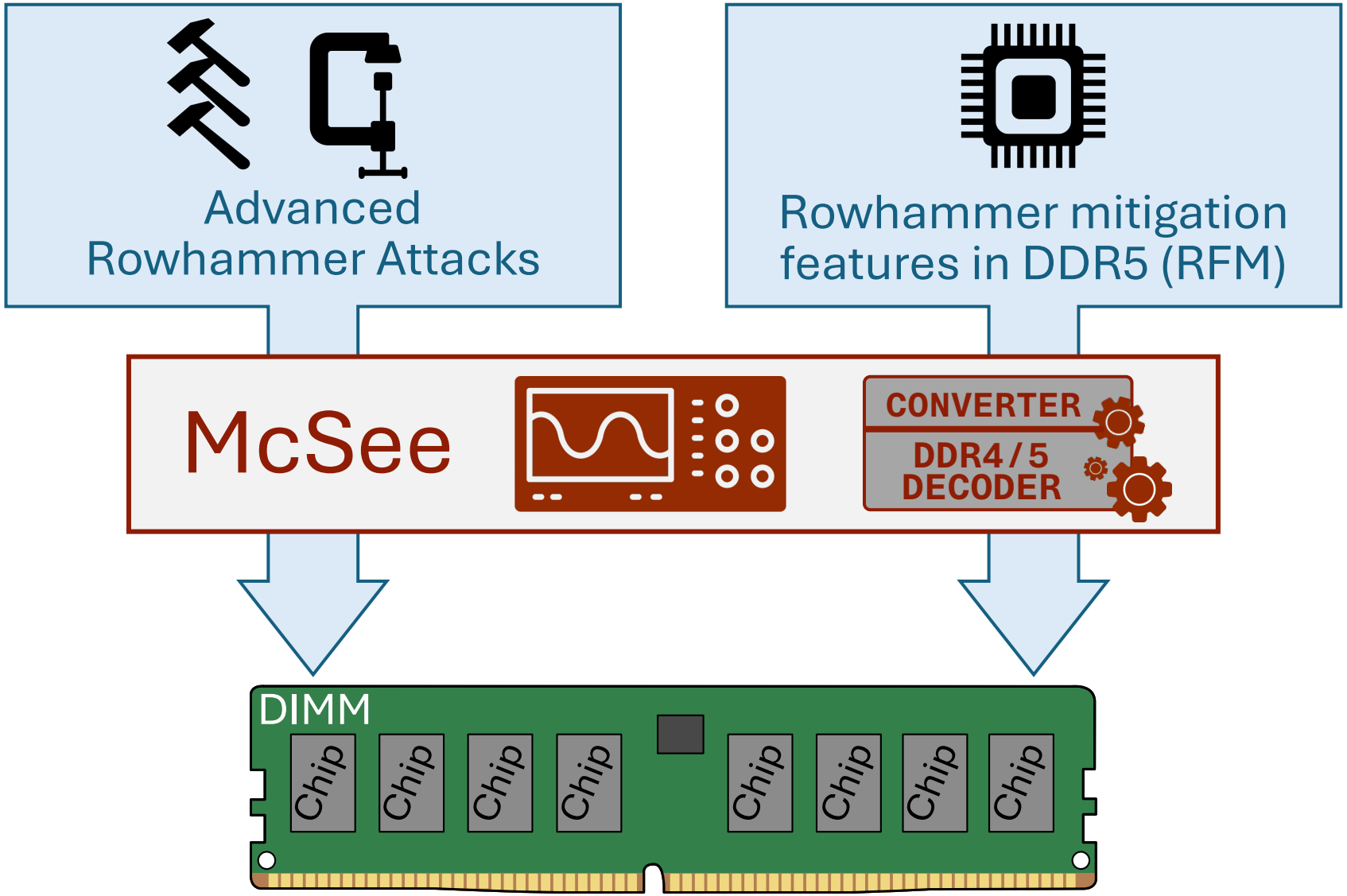
McSee


Advanced
Rowhammer Attacks
DIMM
Chip
Chip
Chip
Chip
Chip
Chip
Chip
Chip

McSee


Advanced
Rowhammer Attacks
Rowhammer mitigation
features in DDR5 (RFM)
DIMM
Chip
Chip
Chip
Chip
Chip
Chip
Chip
Chip

McSee


Advanced
Rowhammer Attacks
Rowhammer mitigation
features in DDR5 (RFM)
McSee
CONVERTER
DDR4/5
DECODER
DIMM
Chip
Chip
Chip
Chip
Chip
Chip
Chip
Chip

Our Solution: The McSee Platform

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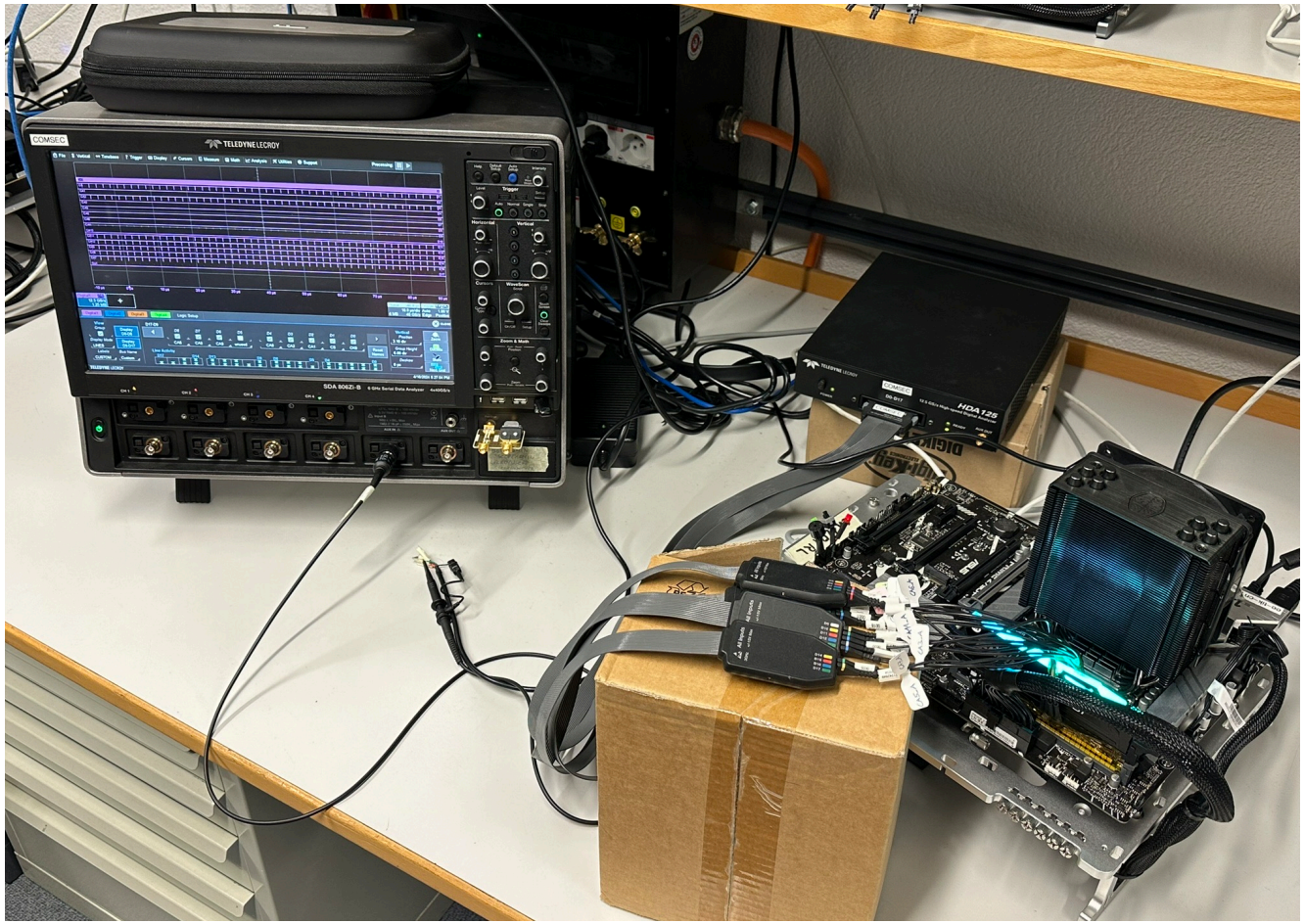


Goals

Requirements
- ≥ 2.4 GHz
- ≥ 16 chs.
- scriptable

Suitable

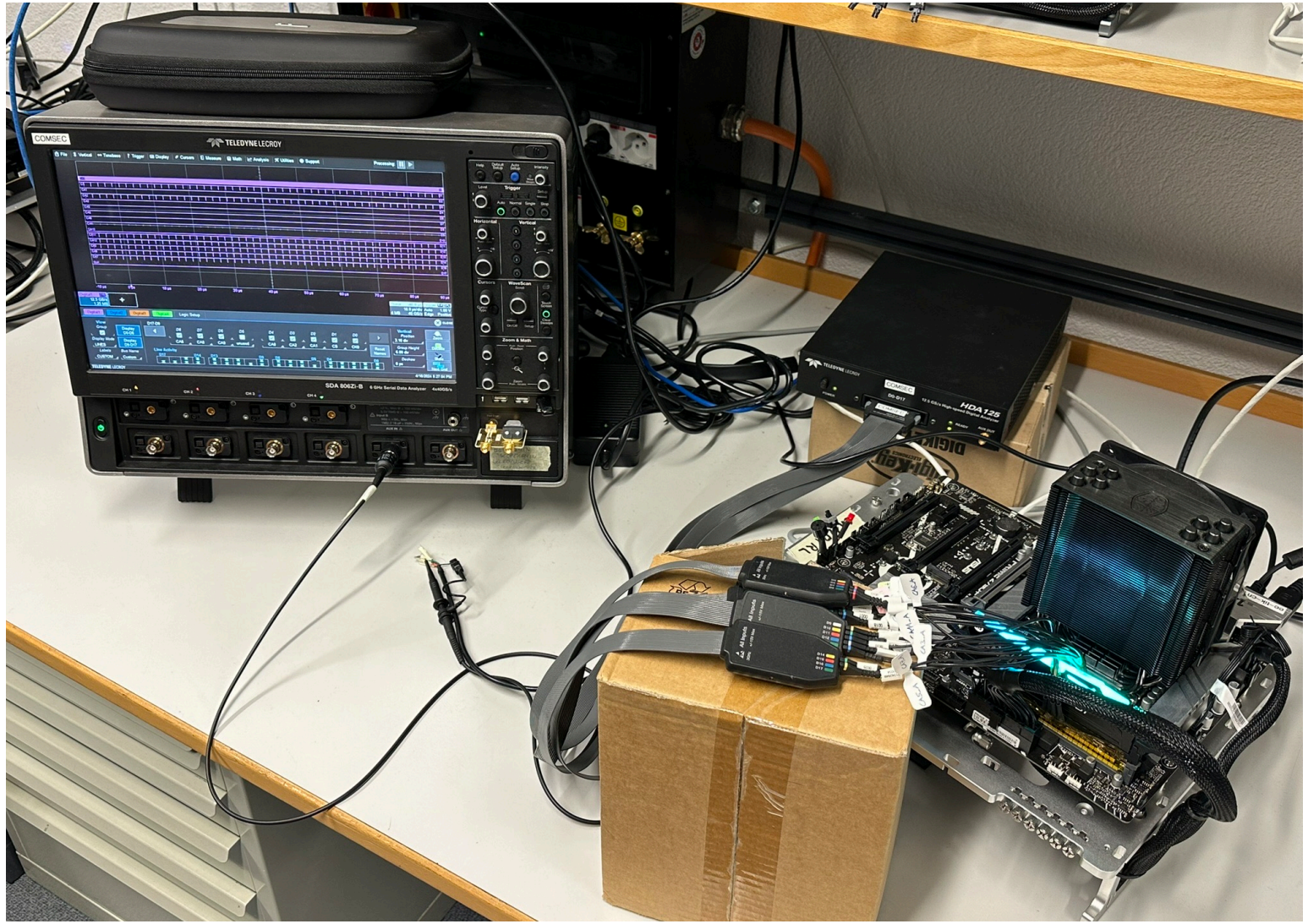
U R SO DIMM DDR 4 5

Flexible

Accessible

- Enables us to **observe** the DRAM **C/A bus** traffic.
- Supports **18 digital signals.**
- Powered by a custom data **processing pipeline**.

Our Solution: The McSee Platform



Component	Model TELEDYNE Name

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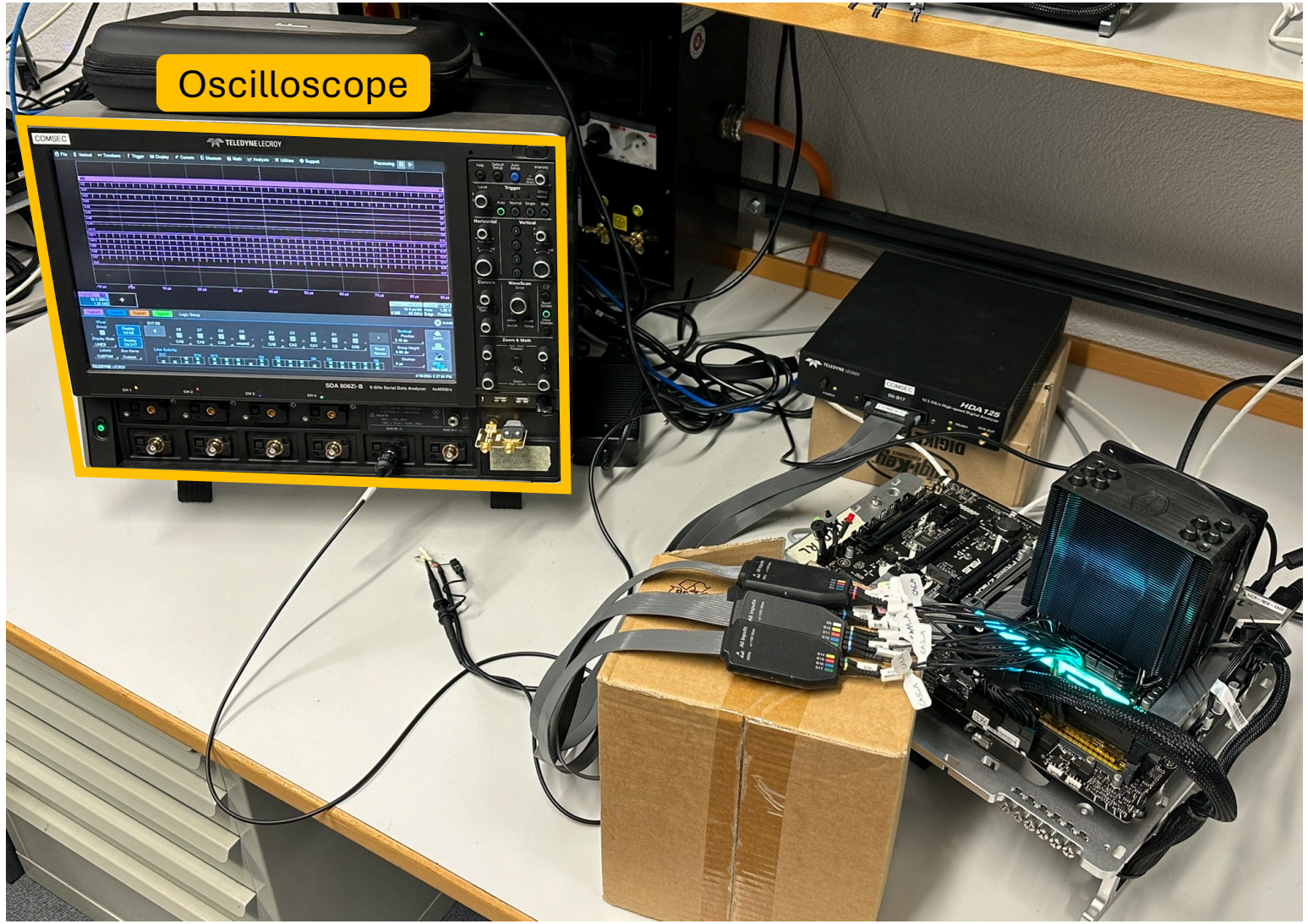

Component	Model TELEDYNE Name
Oscilloscope	SDA 806Zi-B

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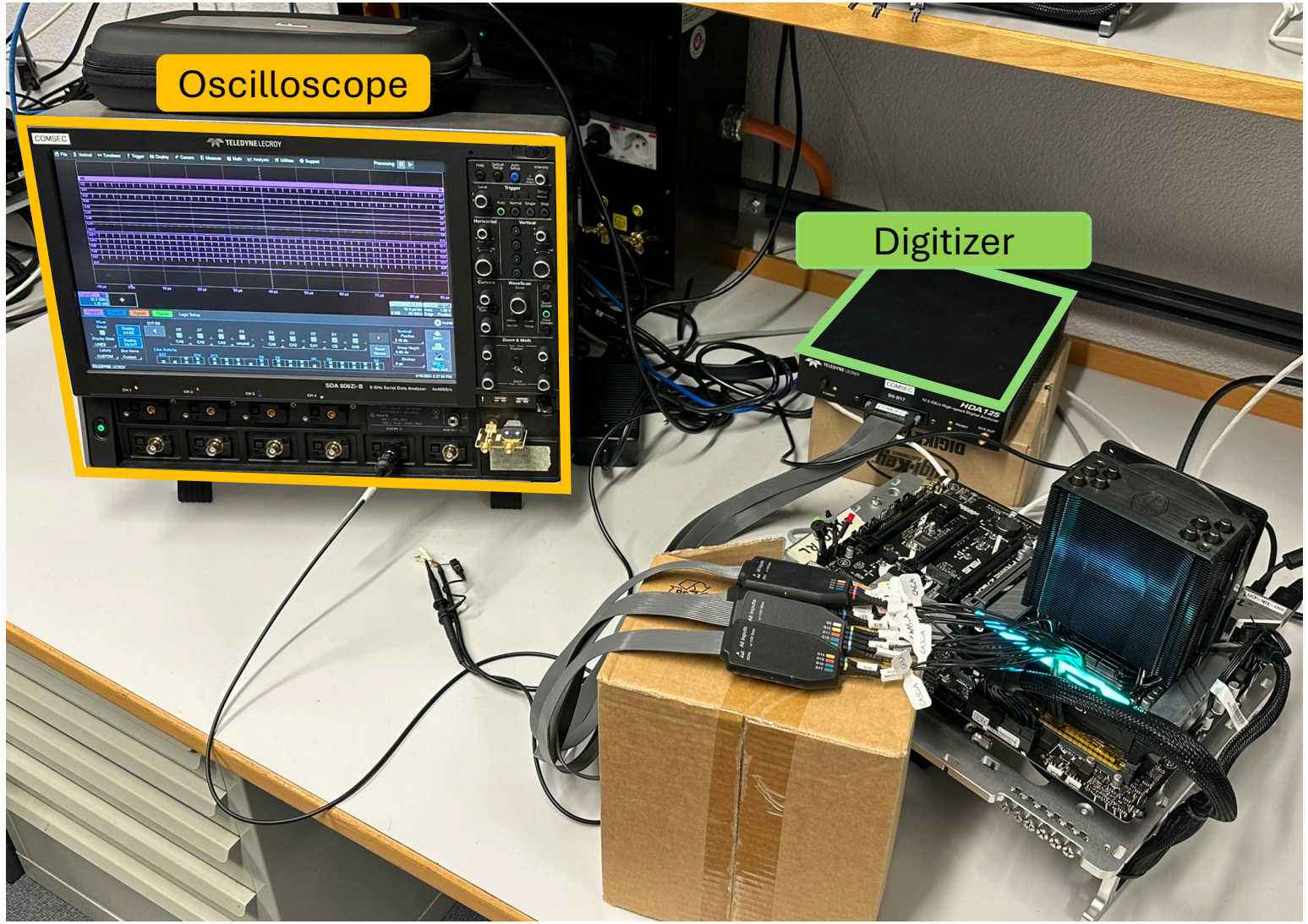

Component	Model TELEDYNE Name
Oscilloscope	SDA 806Zi-B
Digitizer	HDA125-18-LBUS

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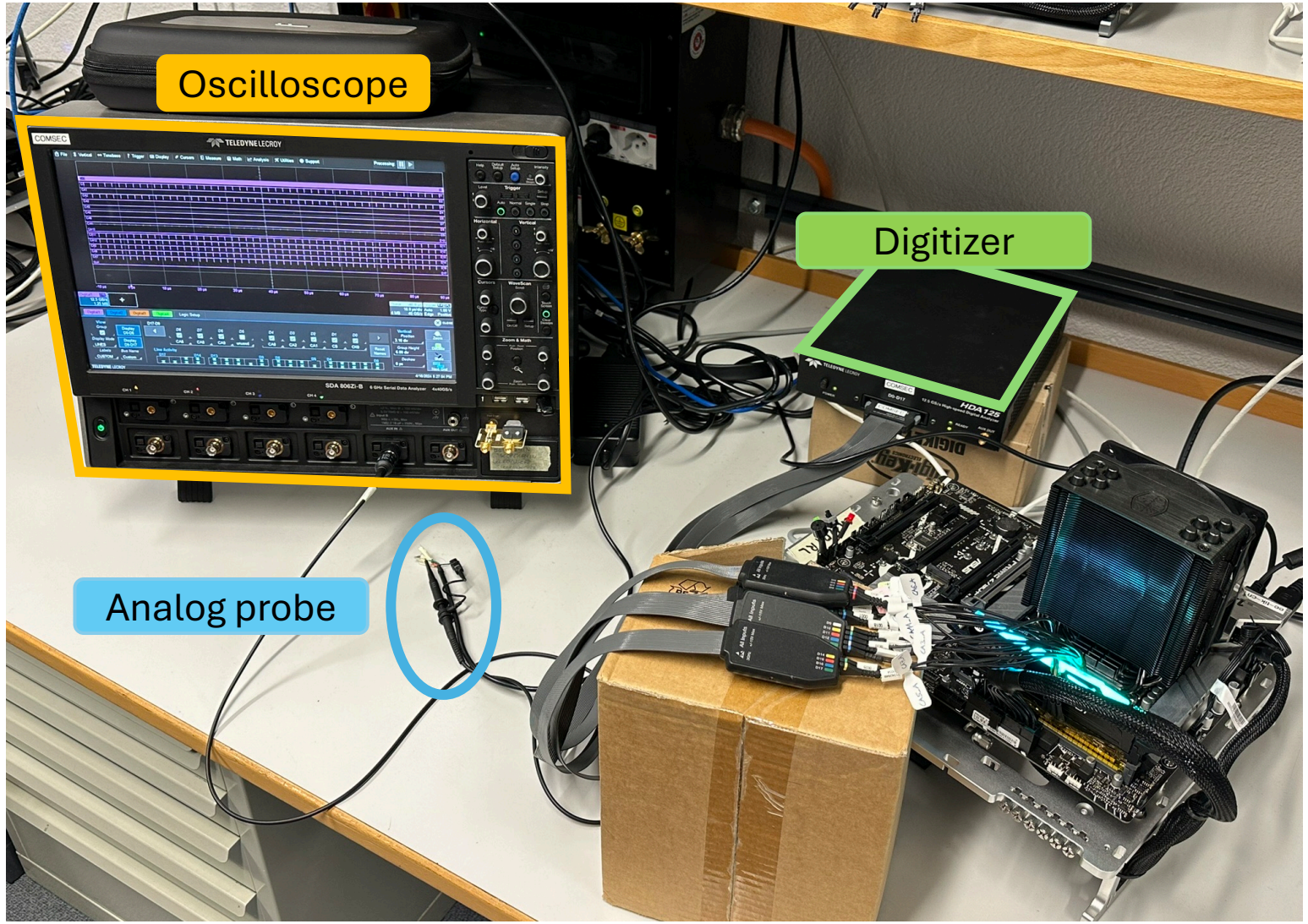

Component	Model TELEDYNE Name
Oscilloscope	SDA 806Zi-B
Digitizer	HDA125-18-LBUS
Analog probe	PP021

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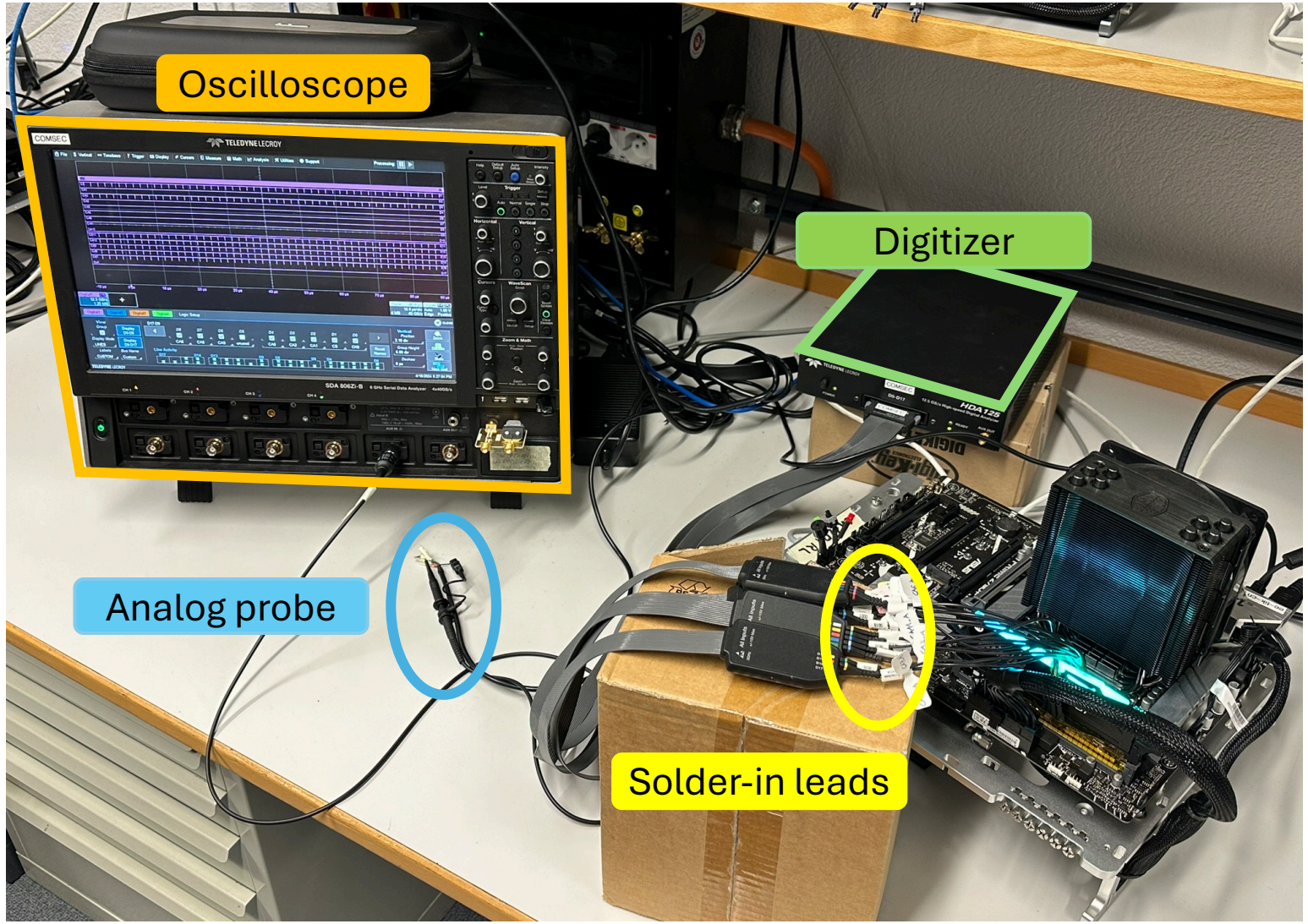

Component	Model TELEDYNE Name
Oscilloscope	SDA 806Zi-B
Digitizer	HDA125-18-LBUS
Analog probe	PP021
Solder-in leads	HAD-DLS-18QL

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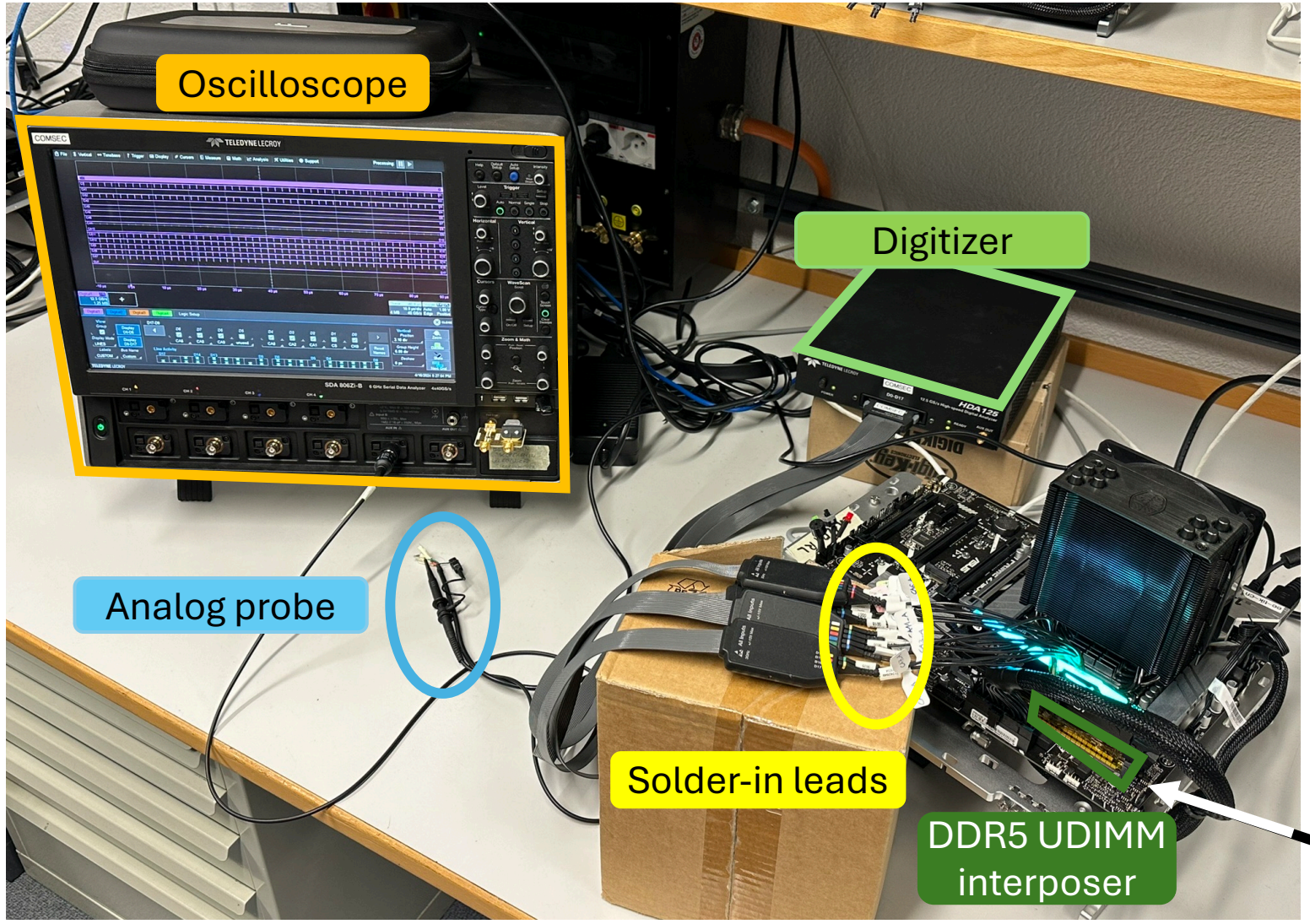
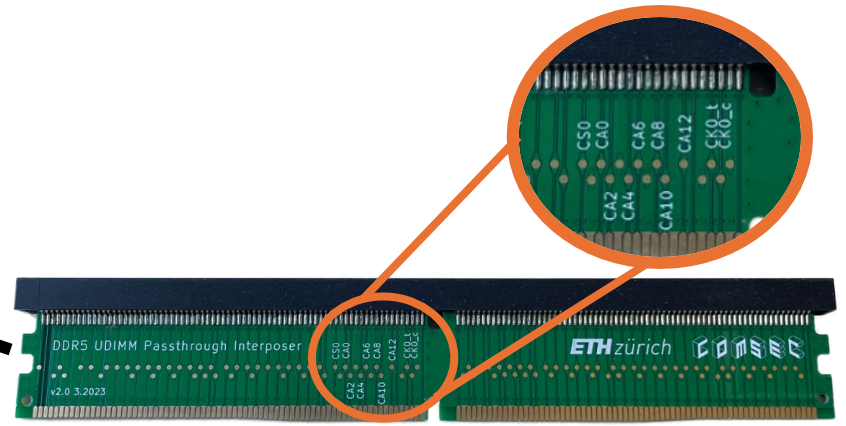
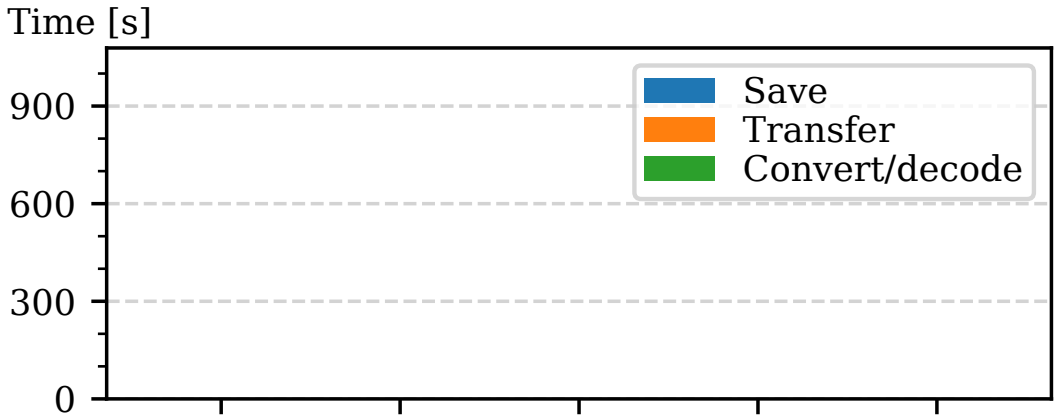


Component	Model TELEDYNE Name
Oscilloscope	SDA 806Zi-B
Digitizer	HDA125-18-LBUS
Analog probe	PP021
Solder-in leads	HAD-DLS-18QL
DDR5 UDIMM interposer	*n/a (custom PCB)*



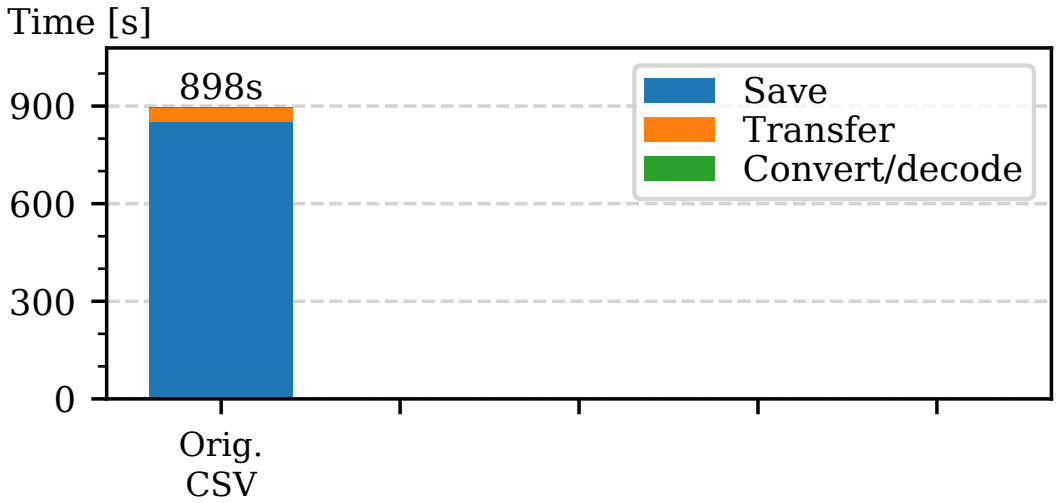
Optimizing McSee

Optimizing McSee



Optimizing McSee

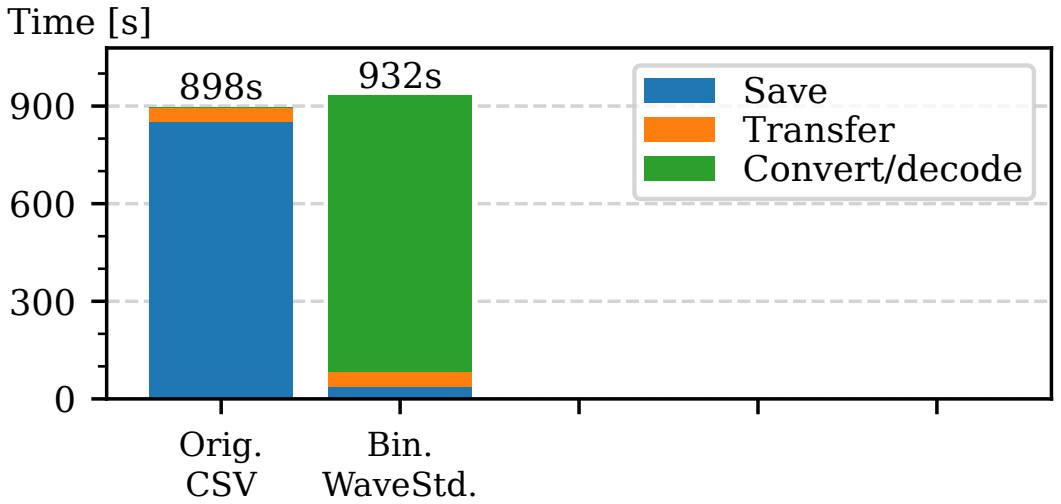
Baseline



Optimizing McSee

Baseline

Bin WaveStudio

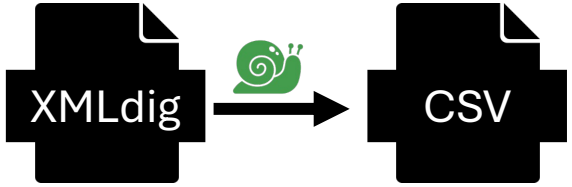


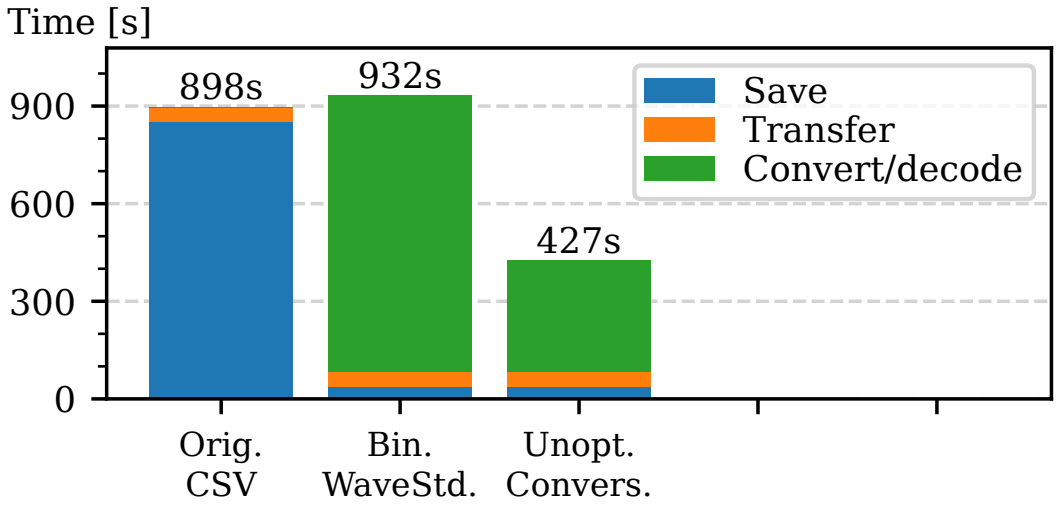
Optimizing McSee

Baseline

Bin WaveStudio

Unoptimized Custom Converter





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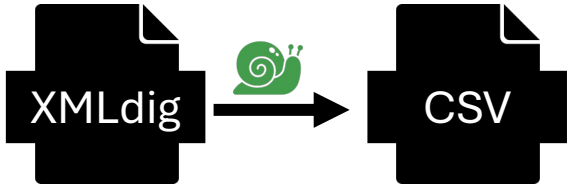
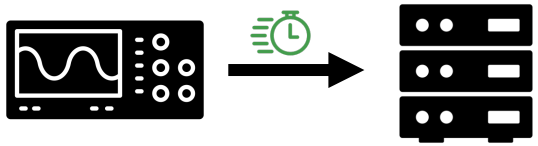
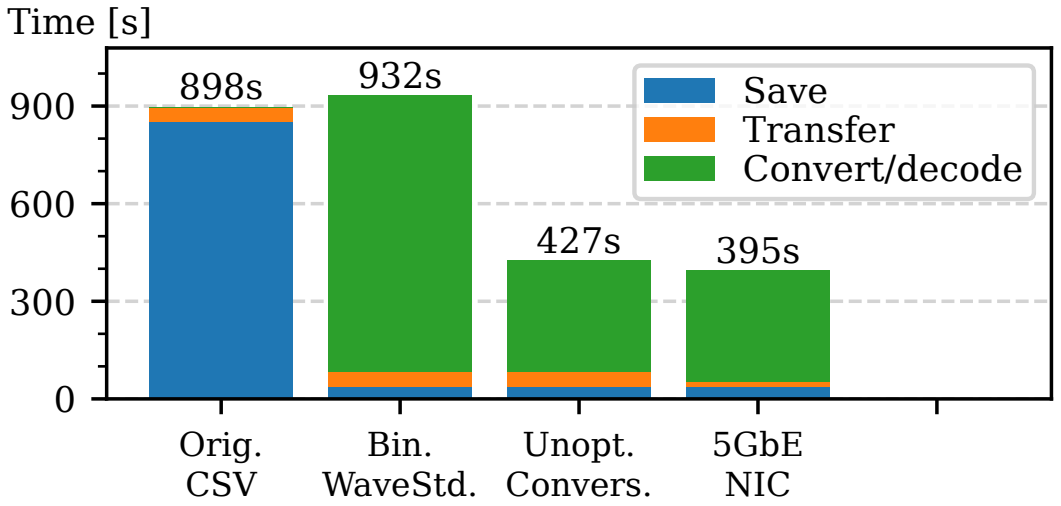


5GbE NIC





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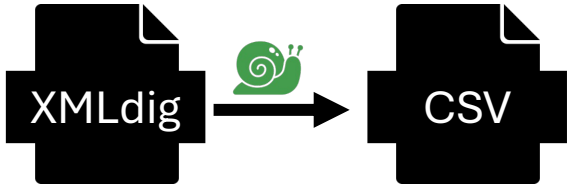

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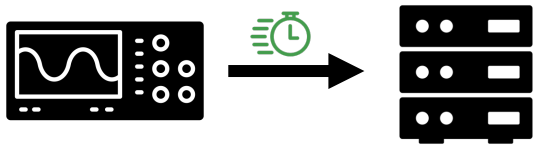
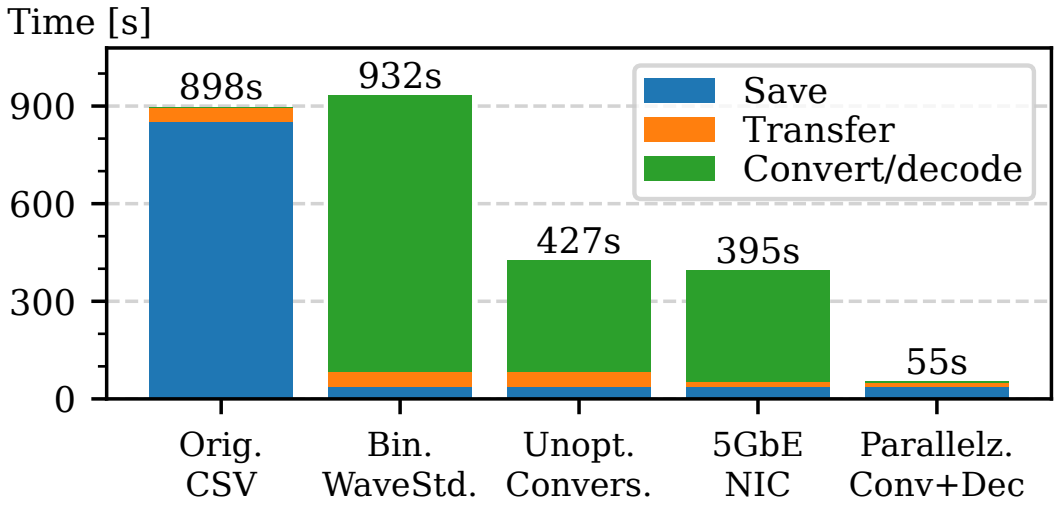


Parallel Conversion & Decoding

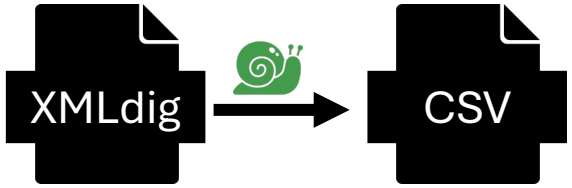


Optimizing McSee

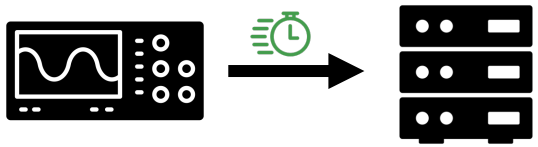
Baseline

Bin WaveStudio

Unoptimized Custom Converter



5GbE NIC



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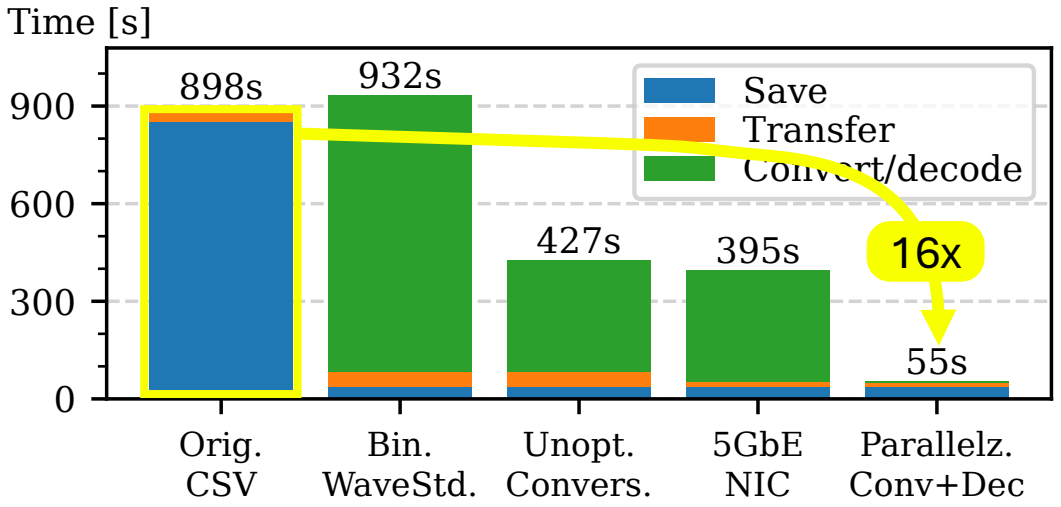
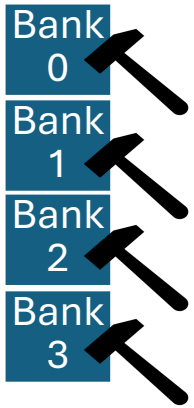


Optimizing the McSee data processing pipeline improved the processing time by 16x.

Analyzing Advanced DRAM Attacks

Analyzing Advanced DRAM Attacks

SledgeHammer: Amplifying Rowhammer via Bank-level Parallelism



Sledgehammer

(USENIX Security ‘24)

Analyzing Advanced DRAM Attacks

Sledgehammer
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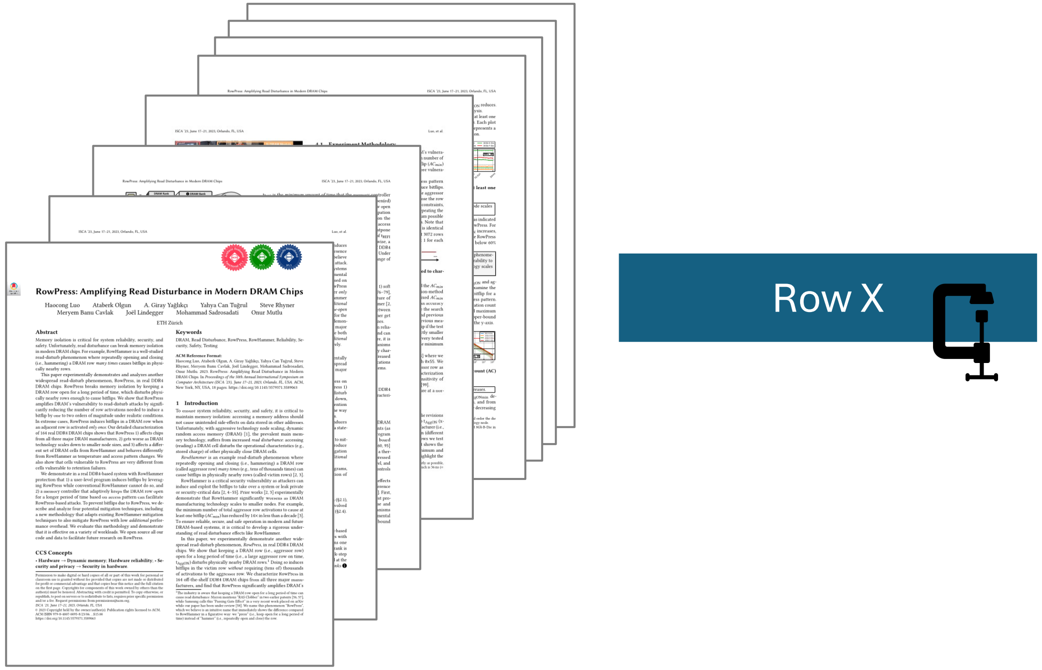
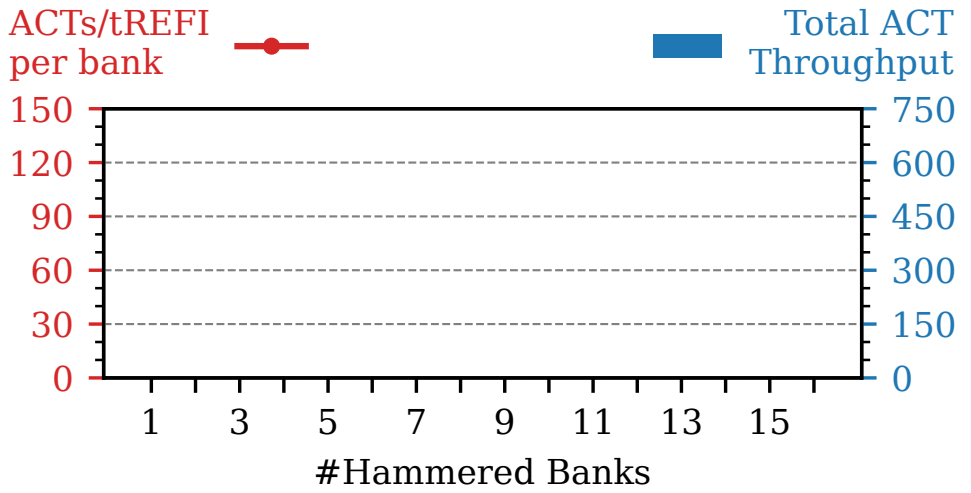


Rowpress
(ISCA ‘24)

Analzying Sledgehammer's ACT Throughput

EXPERIMENT

- Intel i7-8700K (Coffee Lake)
- Run Sledgehammer while hammering **1-16 banks** in parallel.
- Capture traces using McSee.



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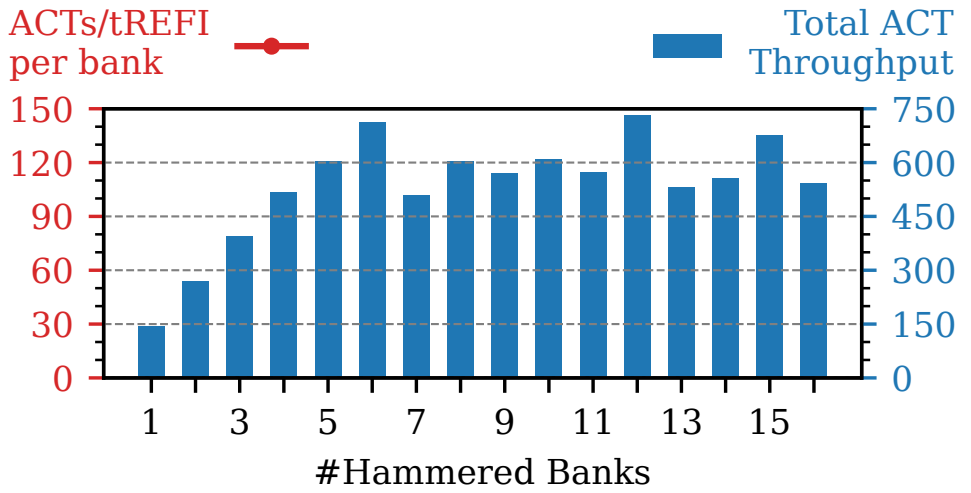

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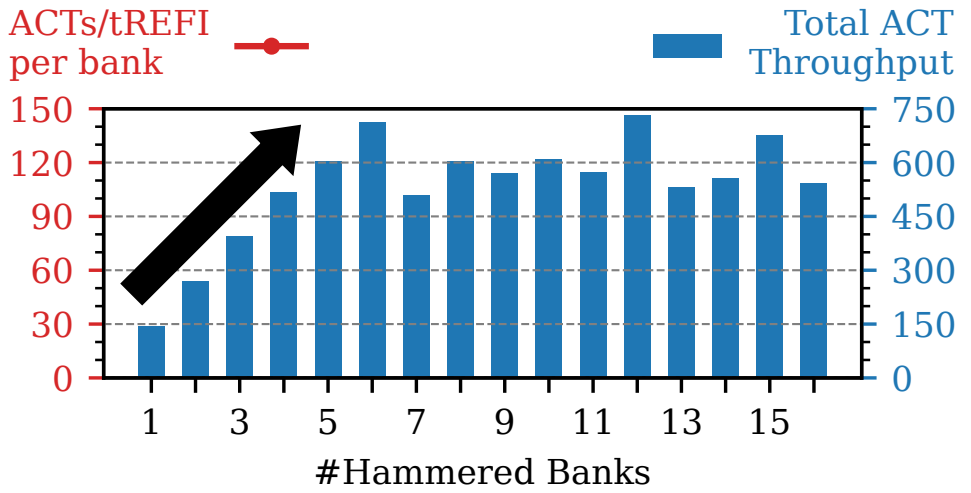

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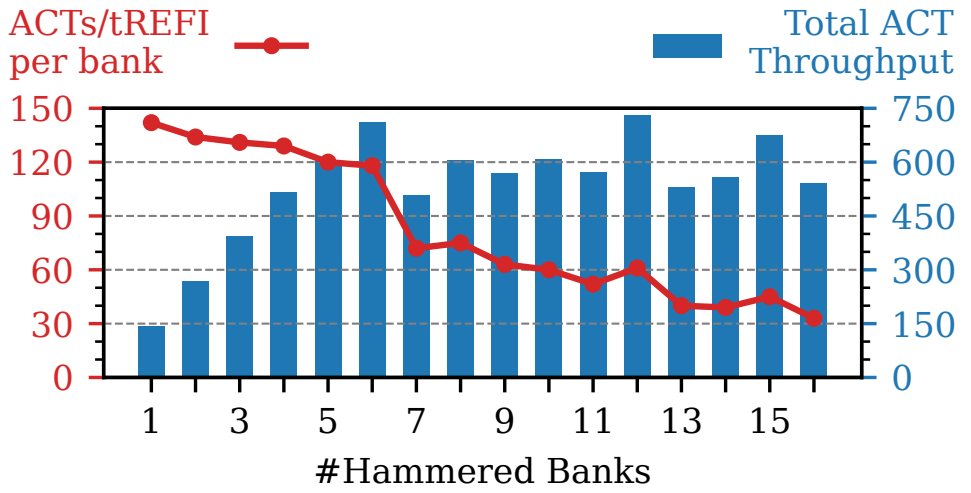

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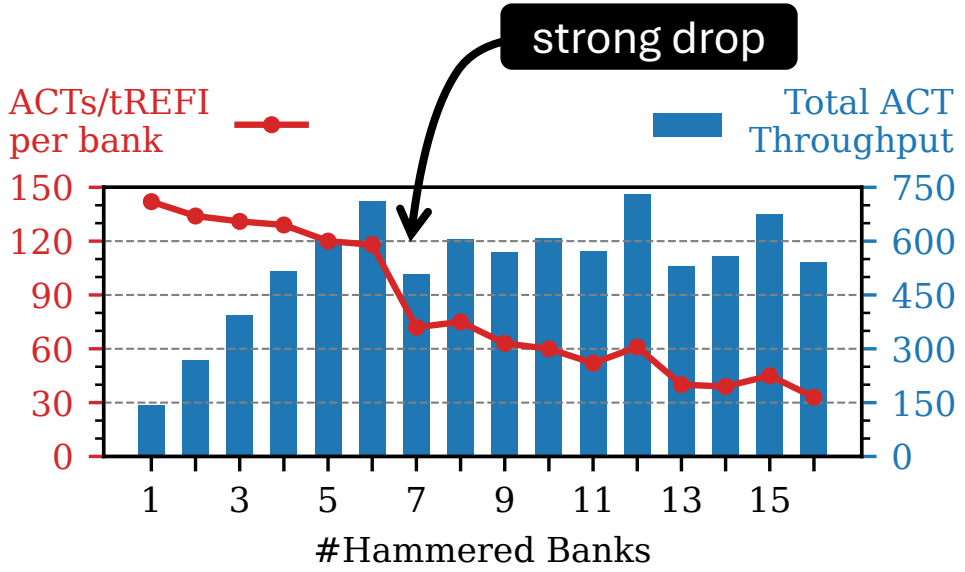

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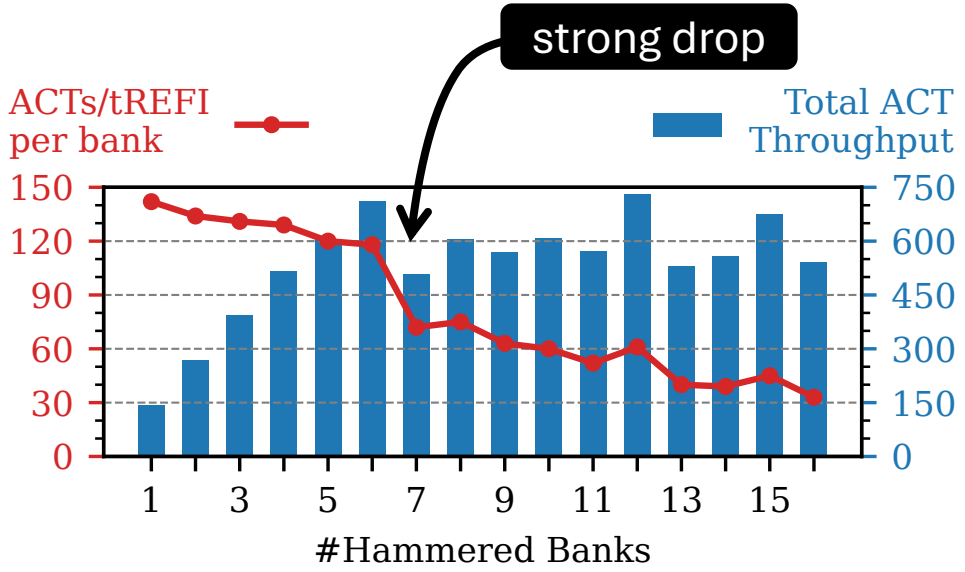

O1. Hammering more banks is beneficial for up to six banks, after which the per-bank ACT rate strongly declines.

Analzying Sledgehammer's ACT Reordering

ANALYSIS

- Hypothesis: more banks hammered ⇒ less ACT reordering.
- Analyze the **ACT-to-ACT distance** of aggressor pairs.

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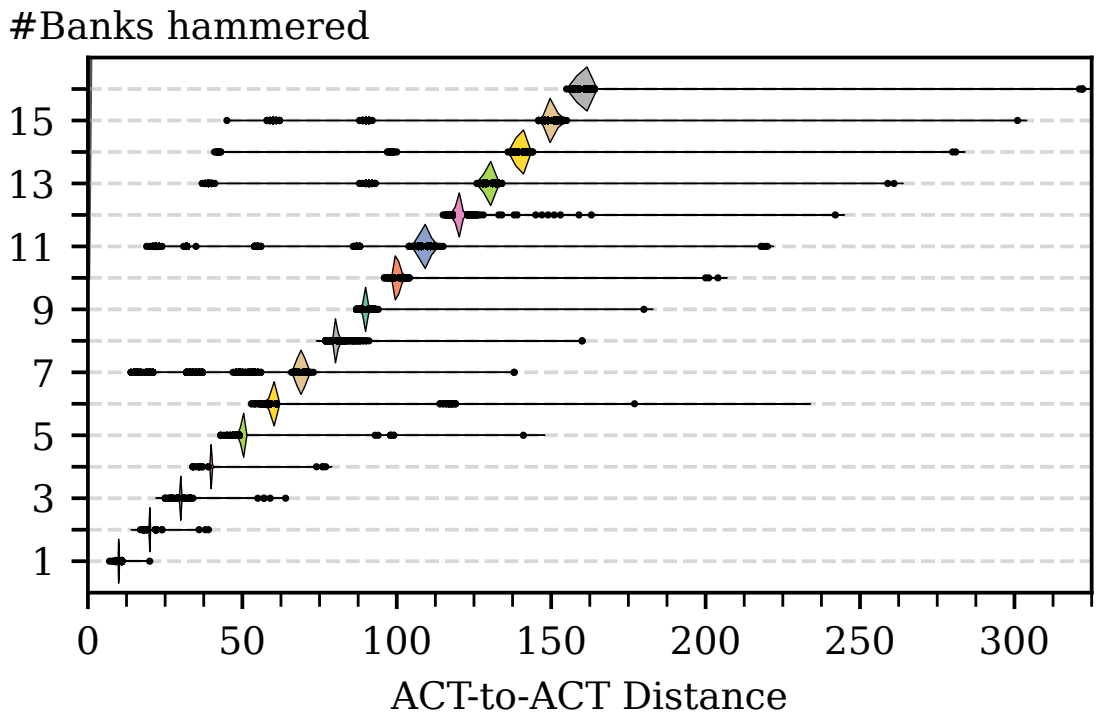

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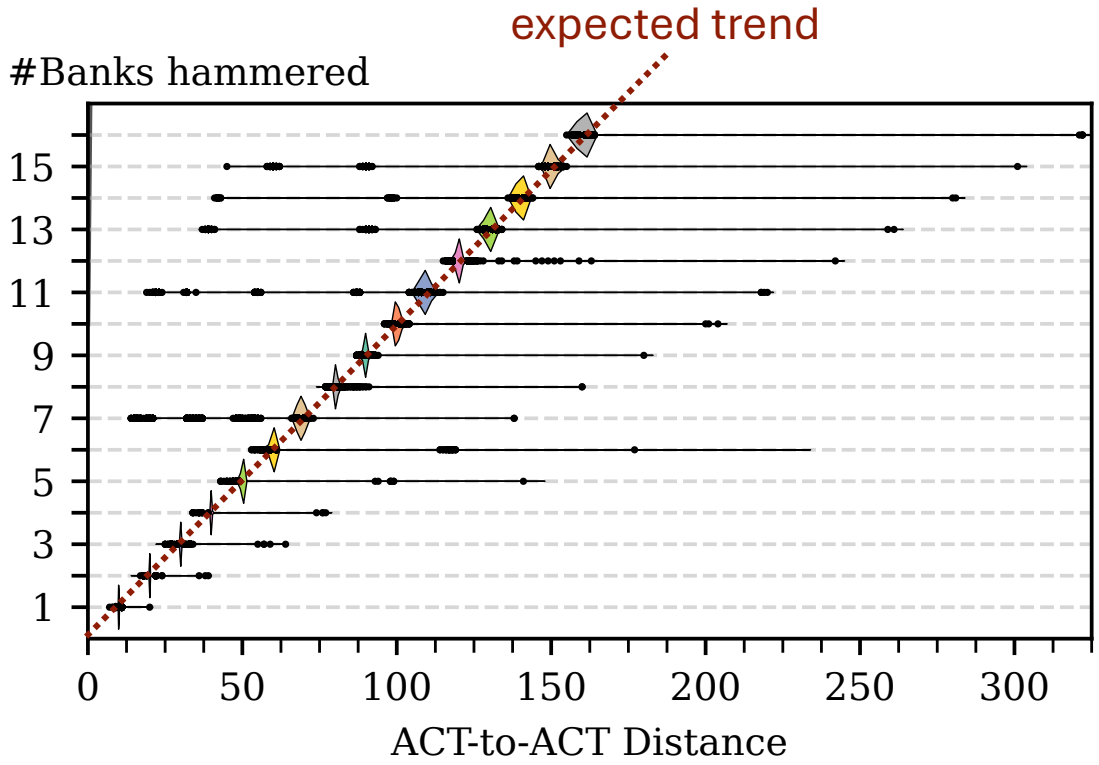

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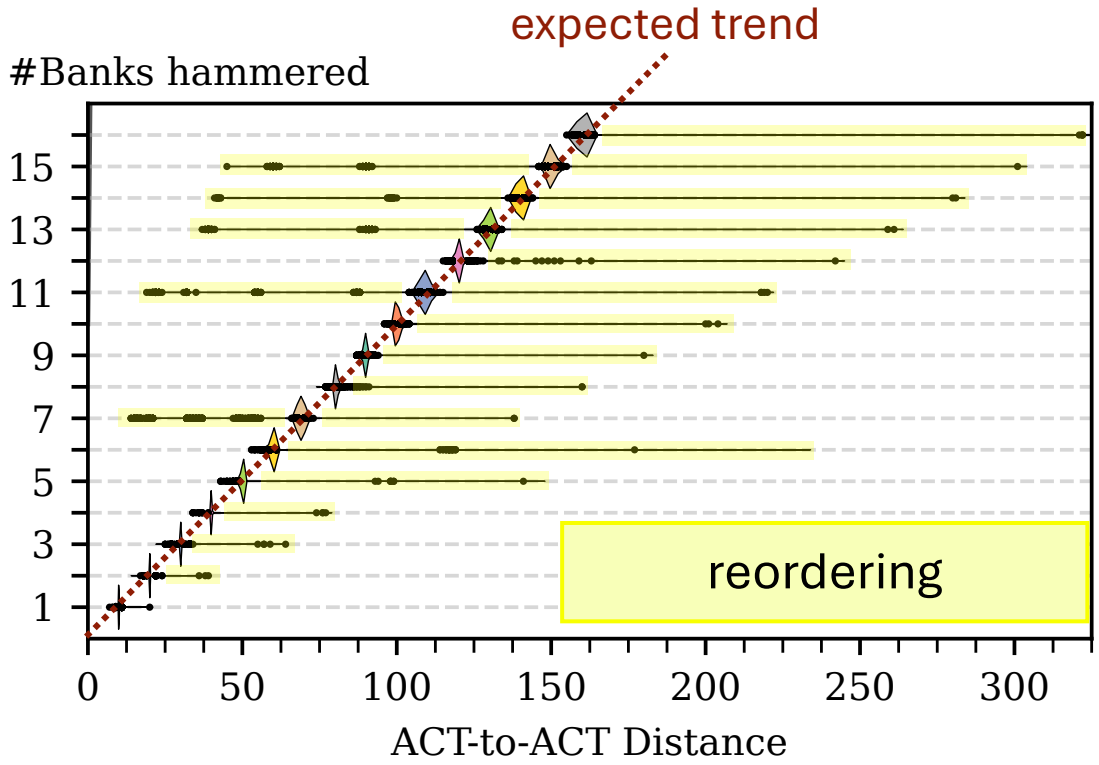

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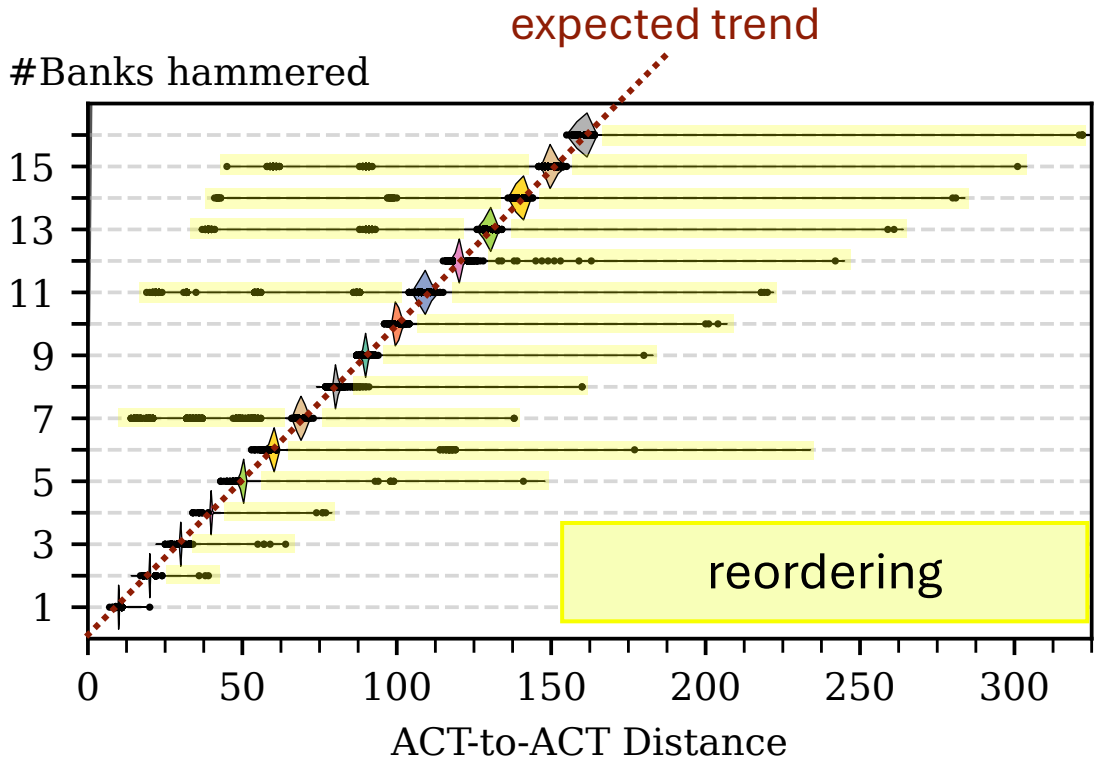

O2. Increasing the number of hammered banks from one to seven causes, on average, 6.7x more reordering of ACTs.

Analzying Rowpress' Row-Open Time

EXPERIMENT

- Intel i7-8700K (Coffee Lake) with same DIMM as org. work.
- Original results reproduced.
- Capture traces while fixing #cache block reads.

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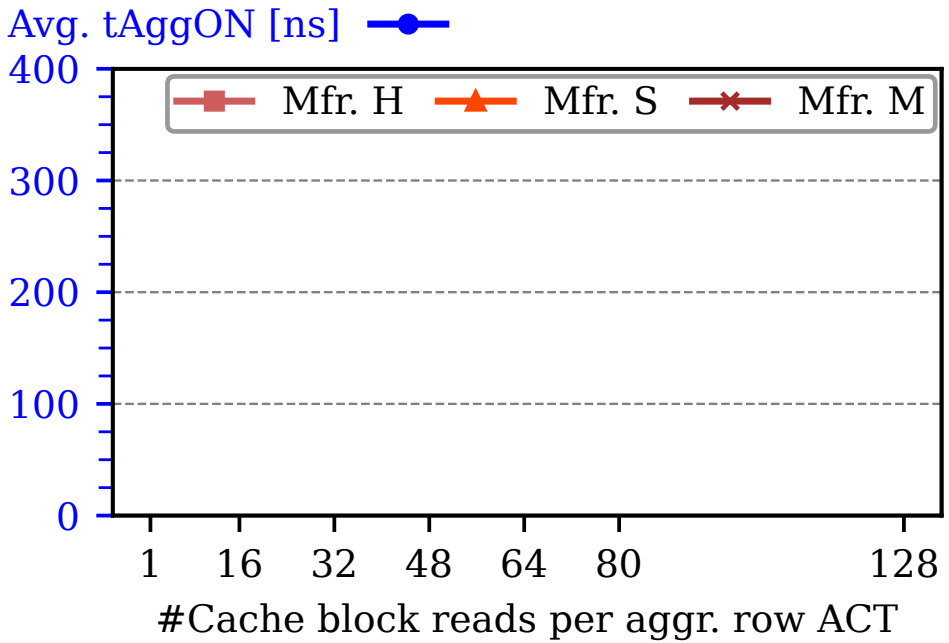

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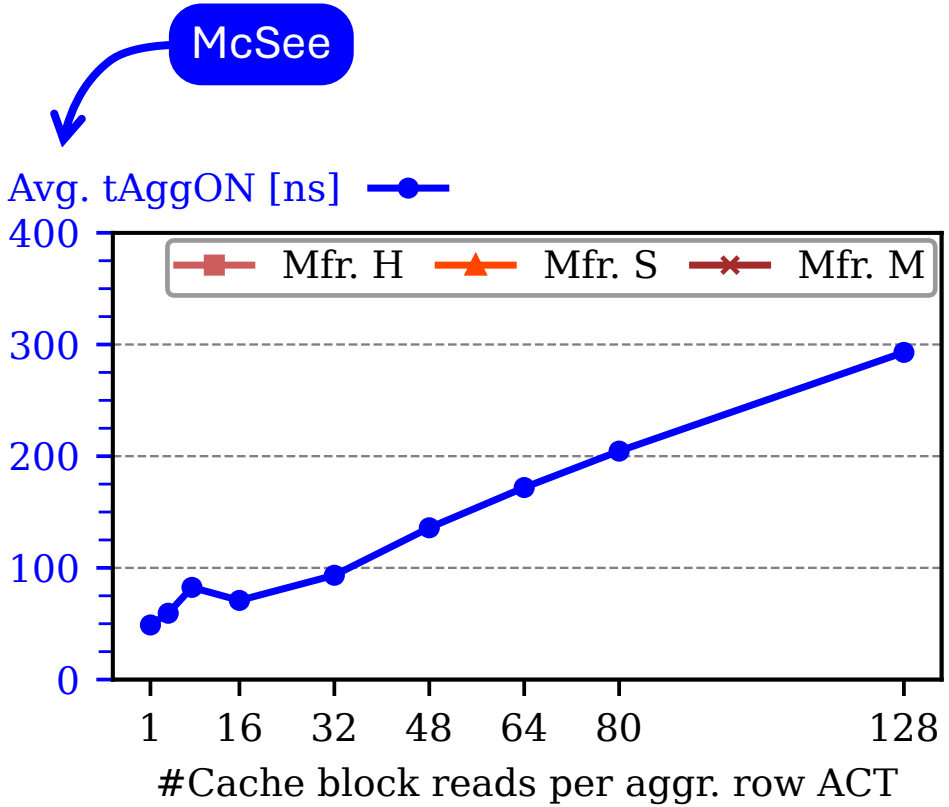

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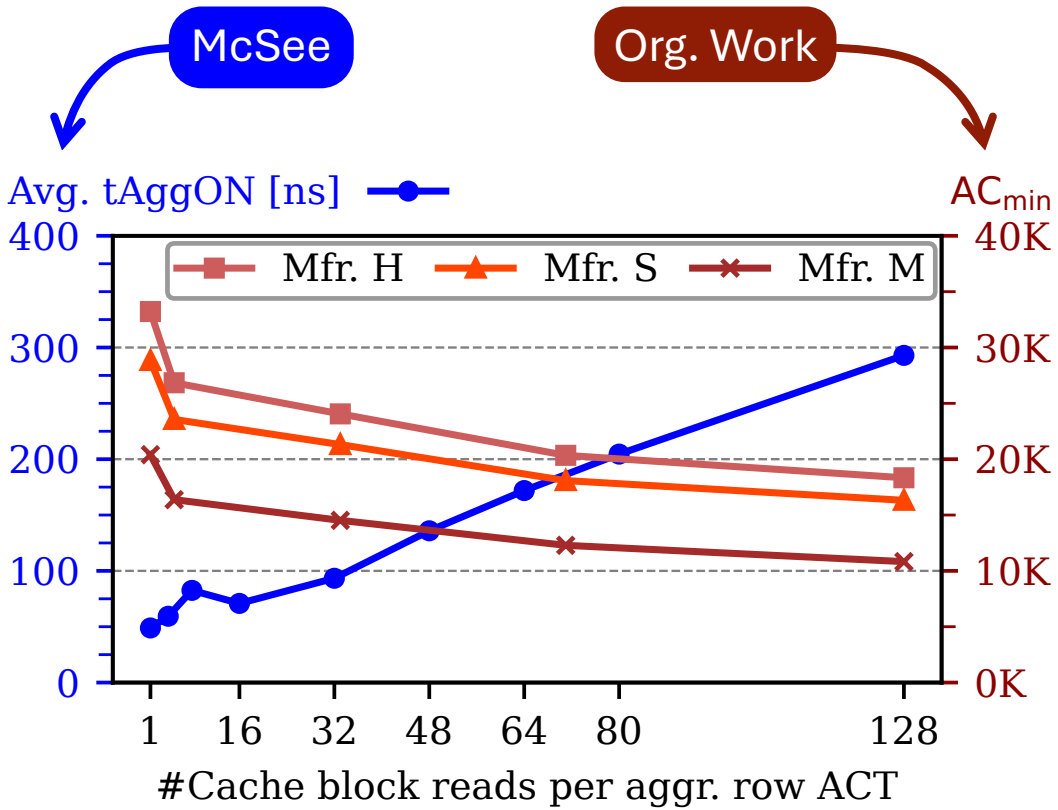

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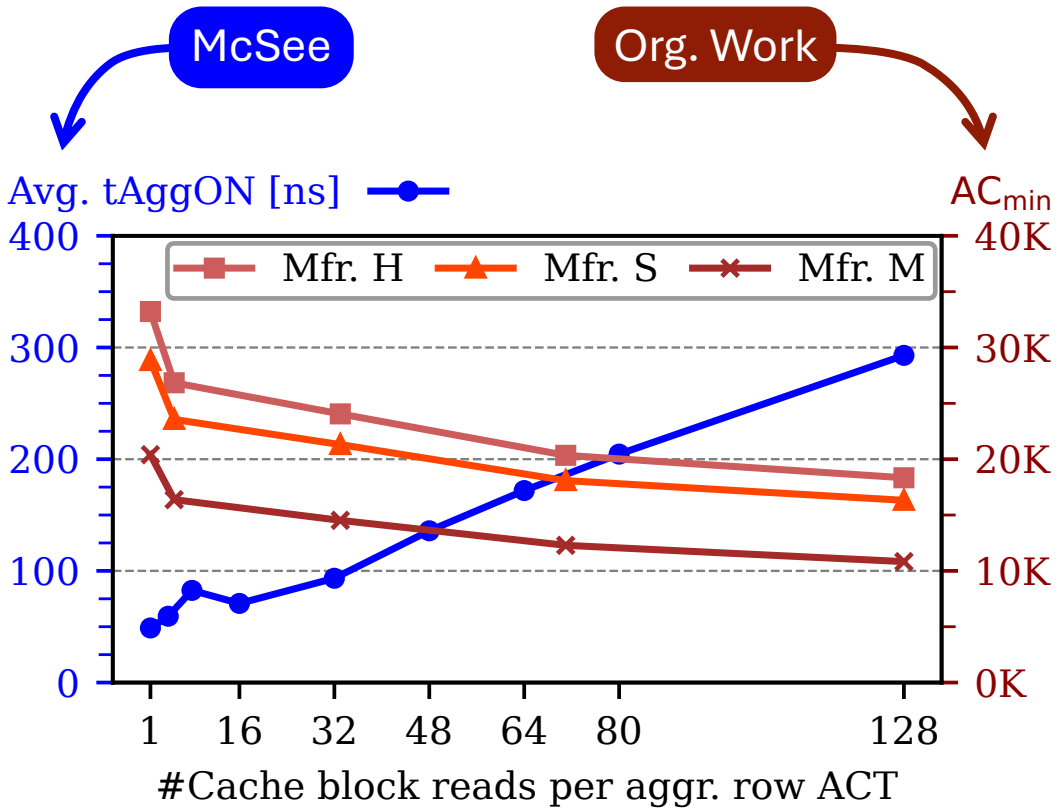
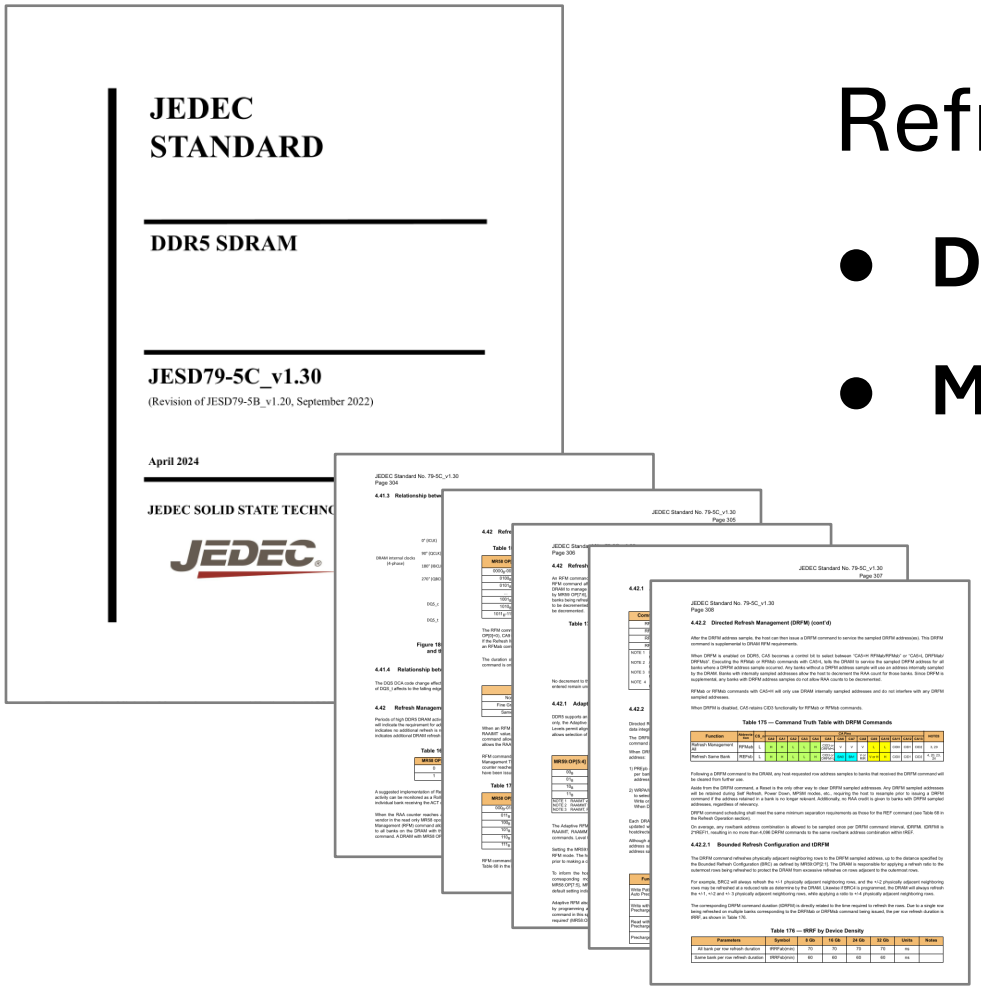


O3. Rowpress' ability to reduce ACmin on commodity systems is significantly lower (2x) than for the most effective pattern (17.6x) in the original work.

Analyzing Rowhammer Defenses



Refresh Management (RFM)

- **DIMM's SPD**: RFM values
- **Memory Controller**: RFM commands

RFM Values

ID	Mf. Date [yy-mm]	Size [GiB]	Wd. [bits]	Geom. #[RK,BK,BA,R]
M1	22-05	16	x8	1,8,4,16
M2	22-08	16	x8	1,8,4,16
M3	22-01	16	x8	1,8,4,16
M4	21-10	16	x8	1,8,4,16
see the results for M5-M11 in the paper				
H1	22-01	8	x16	1,4,4,16
H2	22-12	8	x16	1,4,4,16
H3	22-07	16	x8	1,8,4,16
see the results for H4-H10 in the paper				
H11	21-12	8	X16	1,4,4,16
S1	22-02	8	x16	1,4,4,16
S2	21-12	8	x16	1,4,4,16
S3	22-01	16	x8	1,8,4,16
S4	21-10	16	x8	1,8,4,16
see the results for S5-S7 in the paper				
U1	22-05	8	x16	1,4,4,16

RFM Values

- Custom **DDR5 SPD decoder** to read RFM values:
  - RFM Required
  - RAAIMT
  - RAAMMT

ID	Mf. Date [yy-mm]	Size [GiB]	Wd. [bits]	Geom. #[RK,BK,BA,R]
M1	22-05	16	x8	1,8,4,16
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ID	Mf. Date [yy-mm]	Size [GiB]	Wd. [bits]	Geom. #[RK,BK,BA,R]	RFM [REQ, RAAIMT/-MMT]
M1	22-05	16	x8	1,8,4,16	0, 80, 6x
M2	22-08	16	x8	1,8,4,16	0, RFU, RFU
M3	22-01	16	x8	1,8,4,16	0, 80, 6x
M4	21-10	16	x8	1,8,4,16	0, 80, 4x
see the results for M5-M11 in the paper					
H1	22-01	8	x16	1,4,4,16	0, RFU, RFU
H2	22-12	8	x16	1,4,4,16	0, 80, 6x
H3	22-07	16	x8	1,8,4,16	0, 80, 6x
see the results for H4-H10 in the paper					
H11	21-12	8	X16	1,4,4,16	**1**, 56, 3x
S1	22-02	8	x16	1,4,4,16	0, 80, 6x
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RFM Values

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O5. The majority DDR5 devices report valid RFM values, but only one DIMM requires RFM.

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DDR5 Systems

	Microarchitecture	Release Date	Model
★	Intel **Alder Lake** (AL)	Nov. 2021	i7-12700K
	Intel **Raptor Lake** (RL)	Oct. 2022	i7-13700K
★	AMD **Zen 4** (Z4)	Sept. 2022	R7 7700X

★ First Intel and AMD CPUs with DDR5 support.

RFM in DDR5 Memory Controllers

EXPERIMENT

- Double-sided Rowhammer.
- Tested DIMMs:
  - H5 (SKH, RFM required: No)
  - H11 (SKH, RFM required: Yes)

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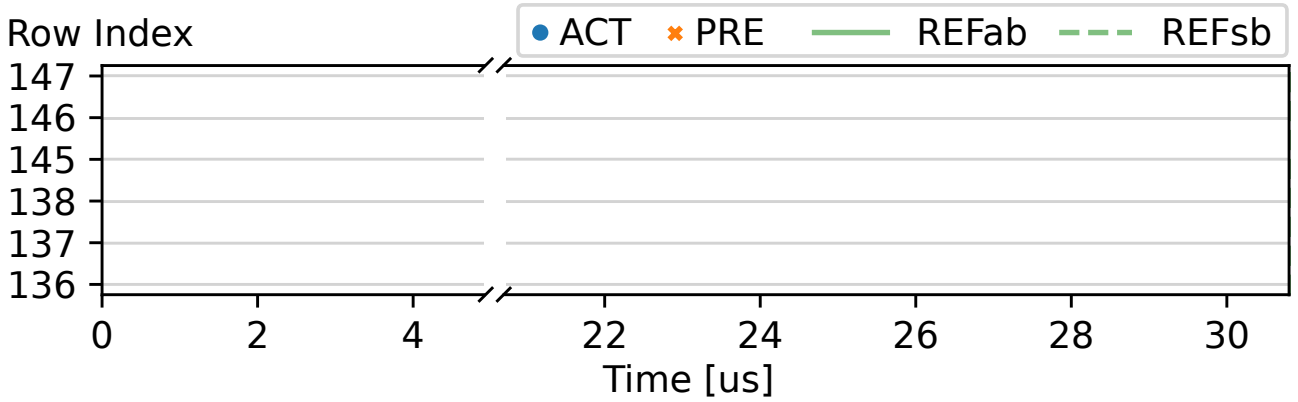

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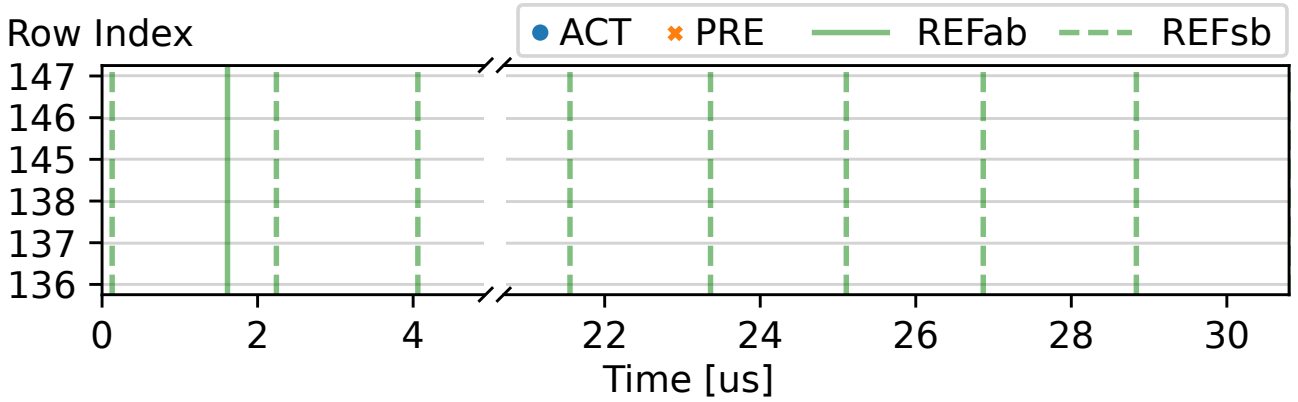

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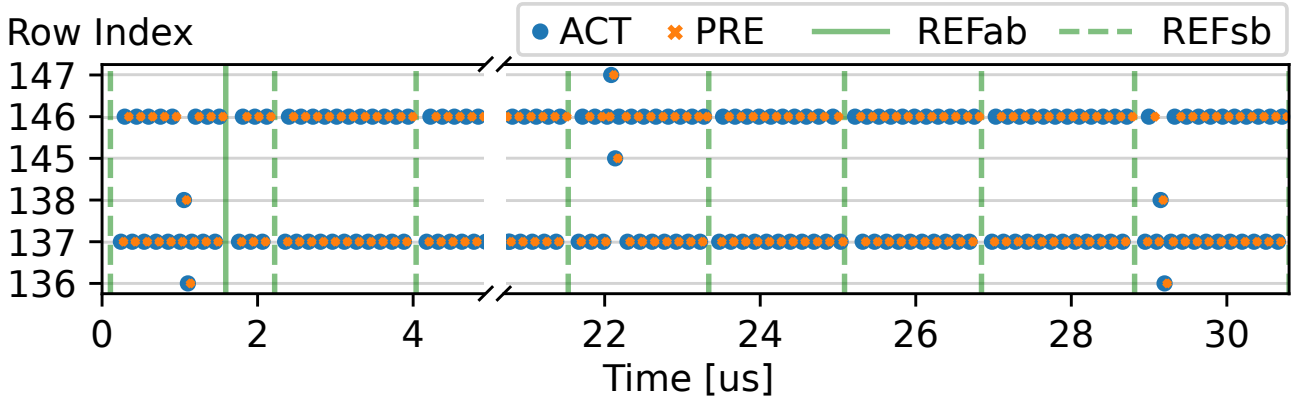

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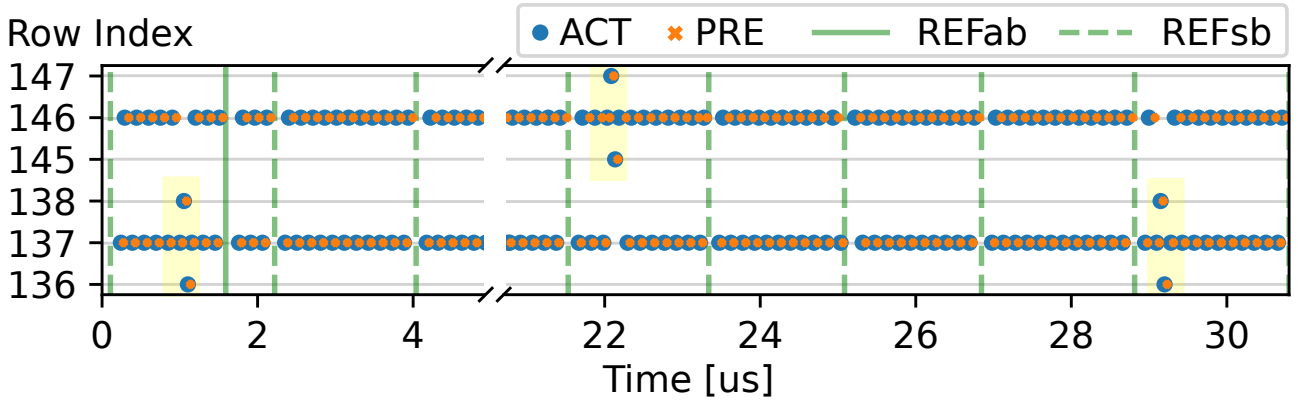

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O9. Intel Raptor Lake CPUs employ pseudo-TRR (pTRR).

Intel’s pseudo-TRR Mitigation

How likely is it that a row gets refreshed by pTRR?

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EXPERIMENT

- Hammer two aggressors for 8192 ACTs.
- `clflush` and `mfence` between hammers.
- Repeat experiment for 512 times.

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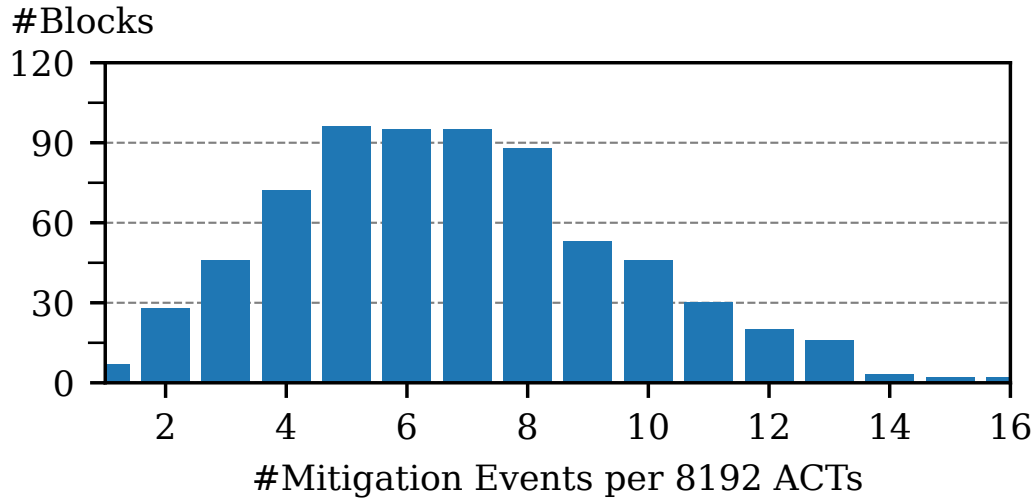

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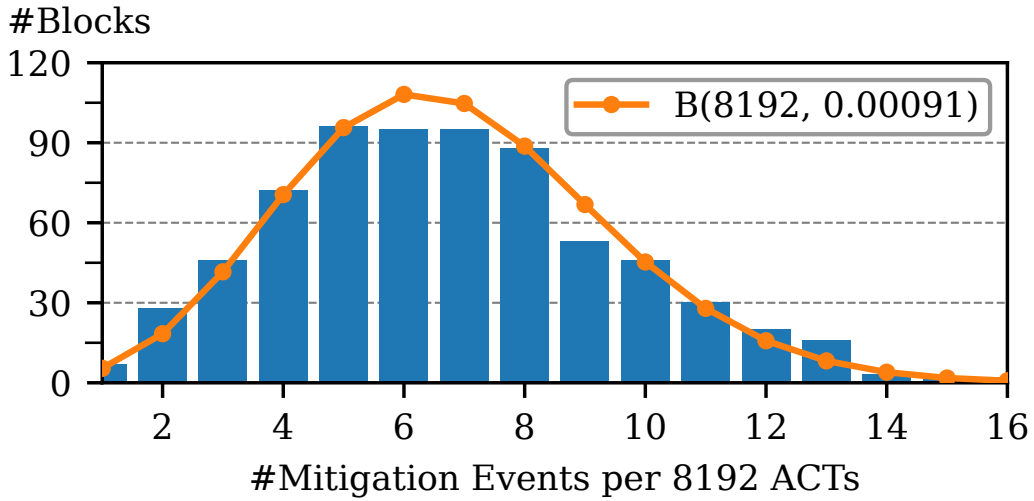

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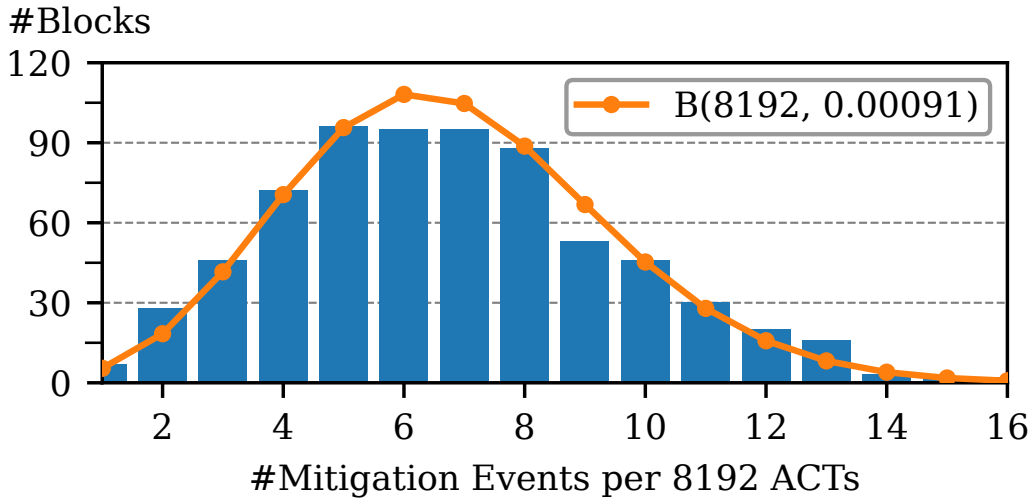


pTRR refreshes aggressor-adjacent rows with a probability of 0.091%.

Intel’s pseudo-TRR Mitigation

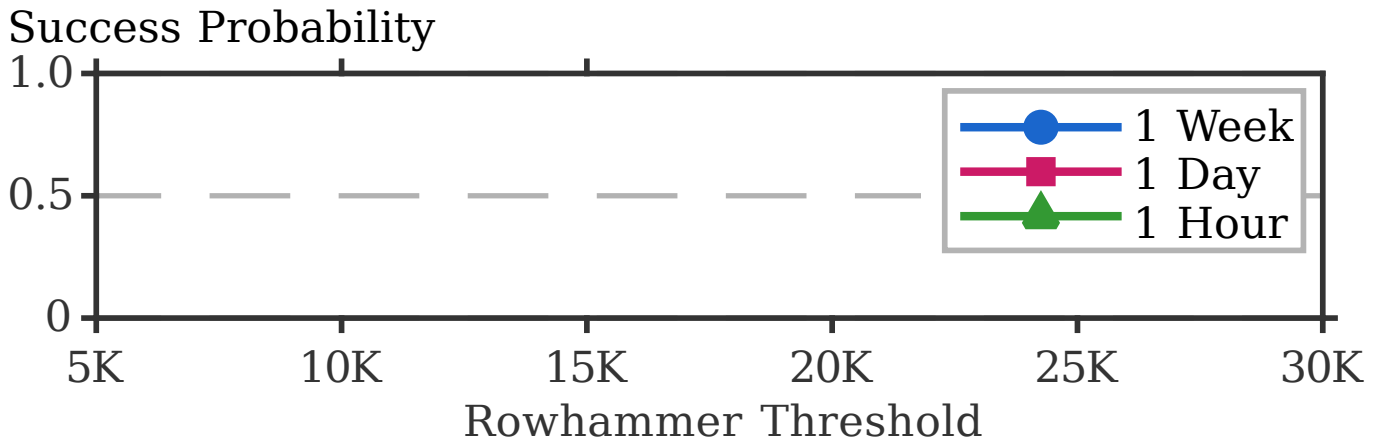
How long does it take to naively bypass pTRR?

[1] A. G. Yağlikçi *et al.*, “HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips,” in *MICRO ’22*, 2022.

Intel's pseudo-TRR Mitigation

How long does it take to naively bypass pTRR?

- PARA model from previous work [1]
- **50%** attack success probability after



[1] A. G. Yağlikçi *et al.*, "HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips," in *MICRO '22*, 2022.

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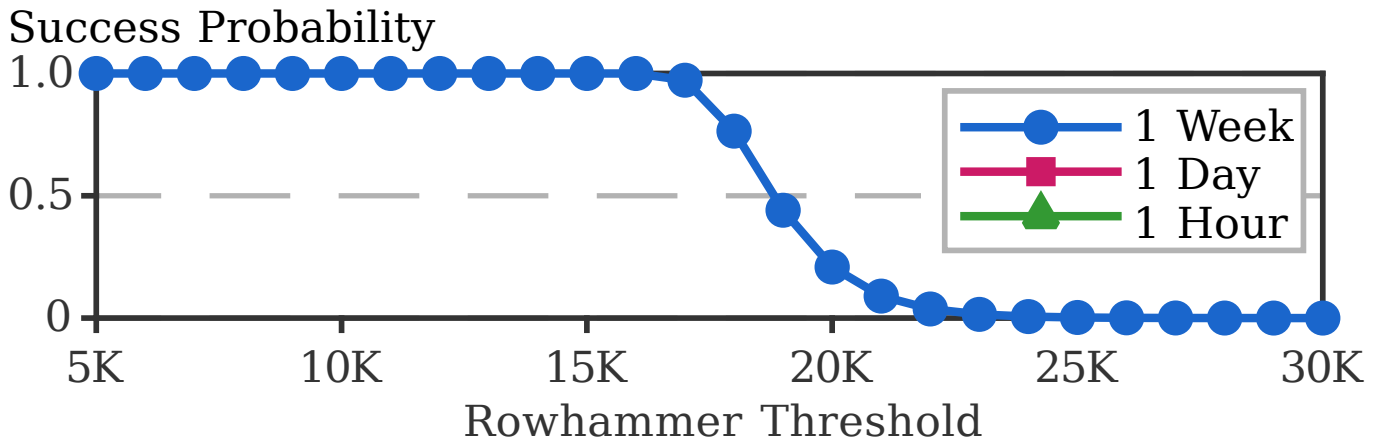

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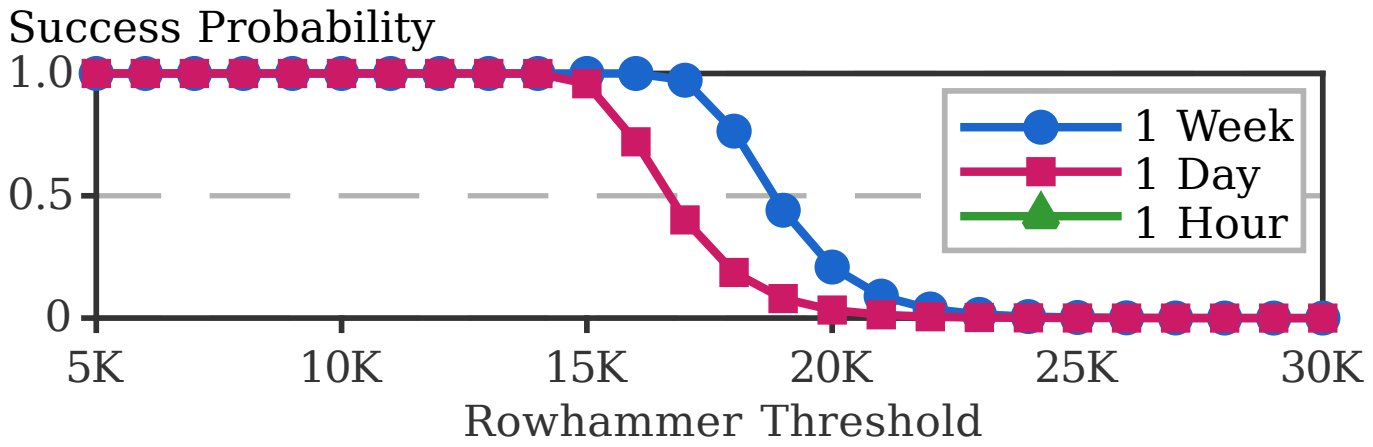

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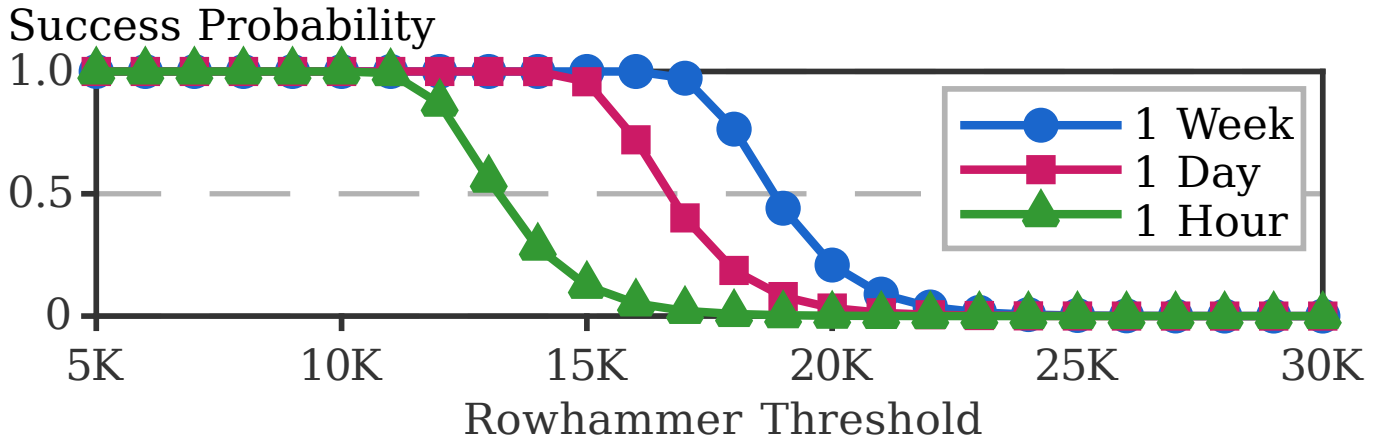

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Future Work

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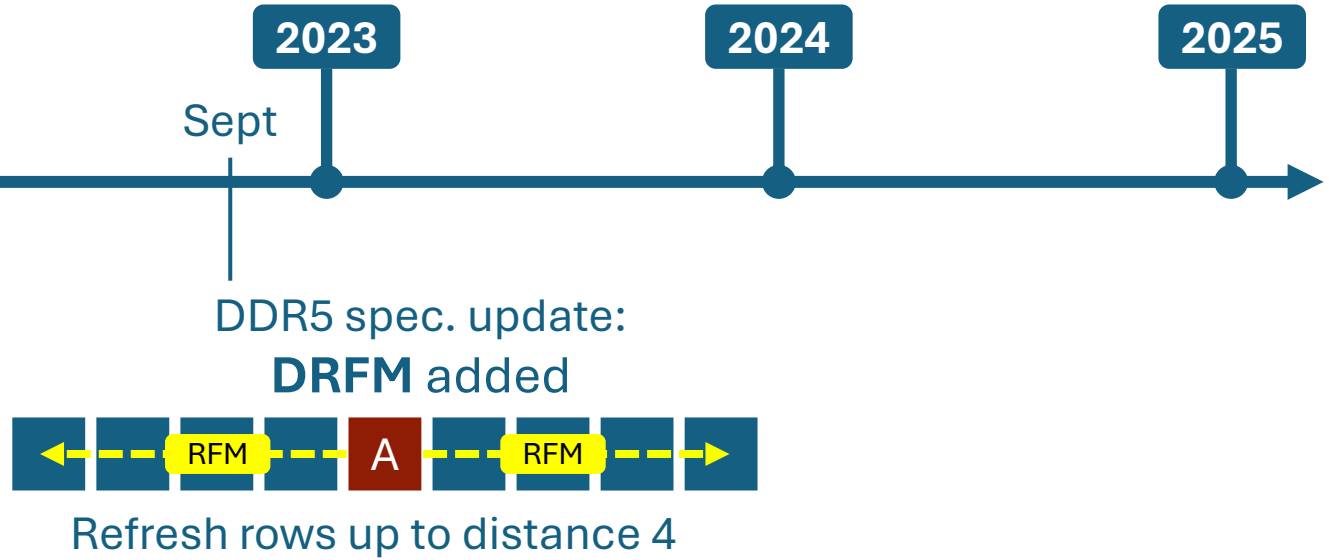
2023
2024
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Sept
DDR5 spec. update:
DRFM added
RFM
A
RFM
Refresh rows up to distance 4

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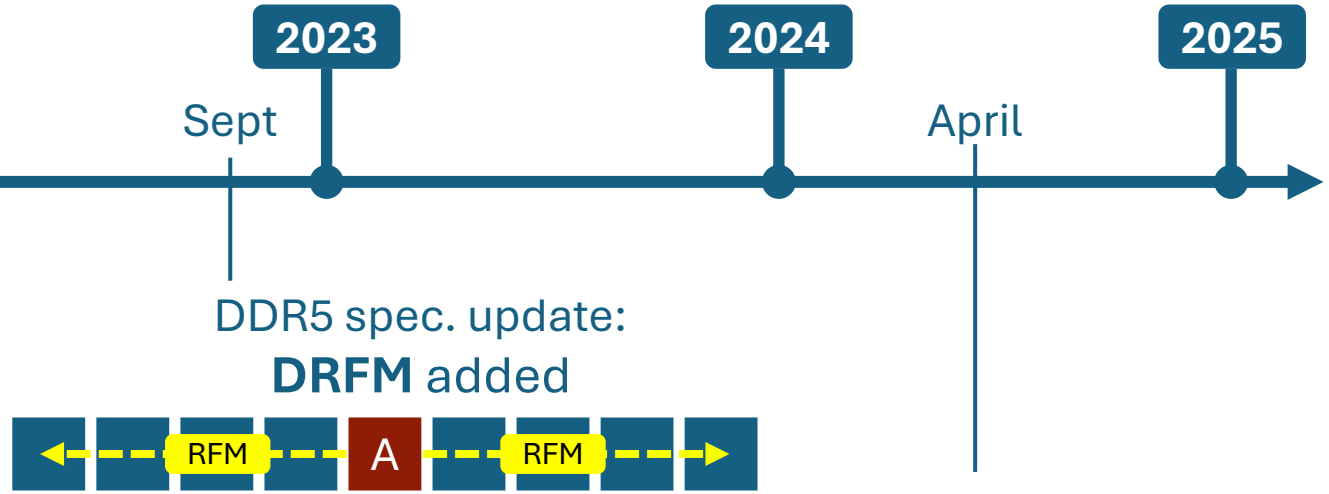
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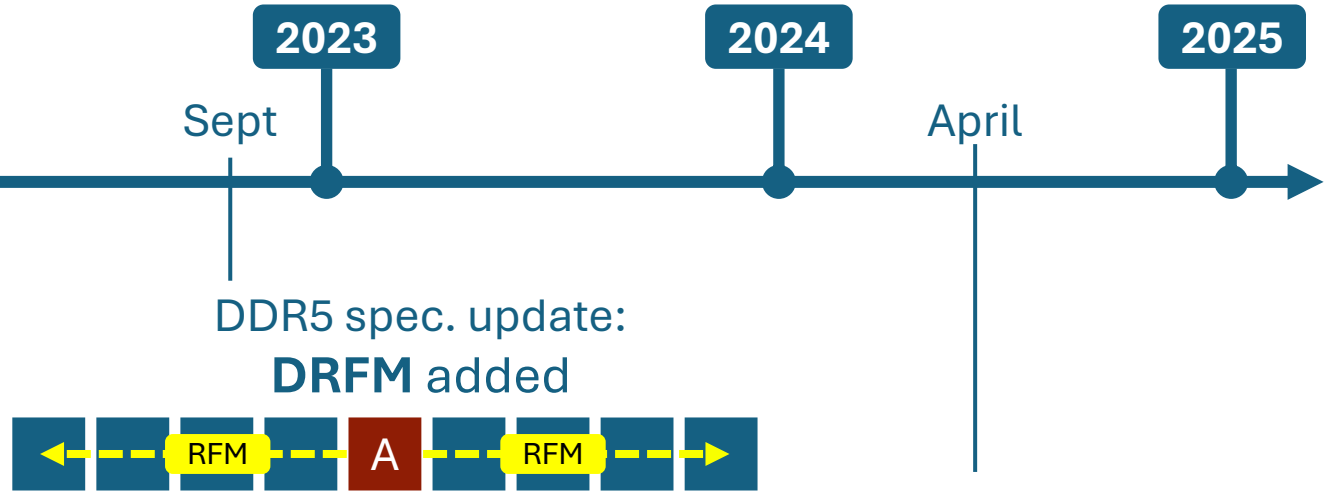
Row 0
#ACTs:
Row 1
#ACTs:
...
Per-row activation counter (DRAM)

Future Work



Improved system-level Rowpress attacks

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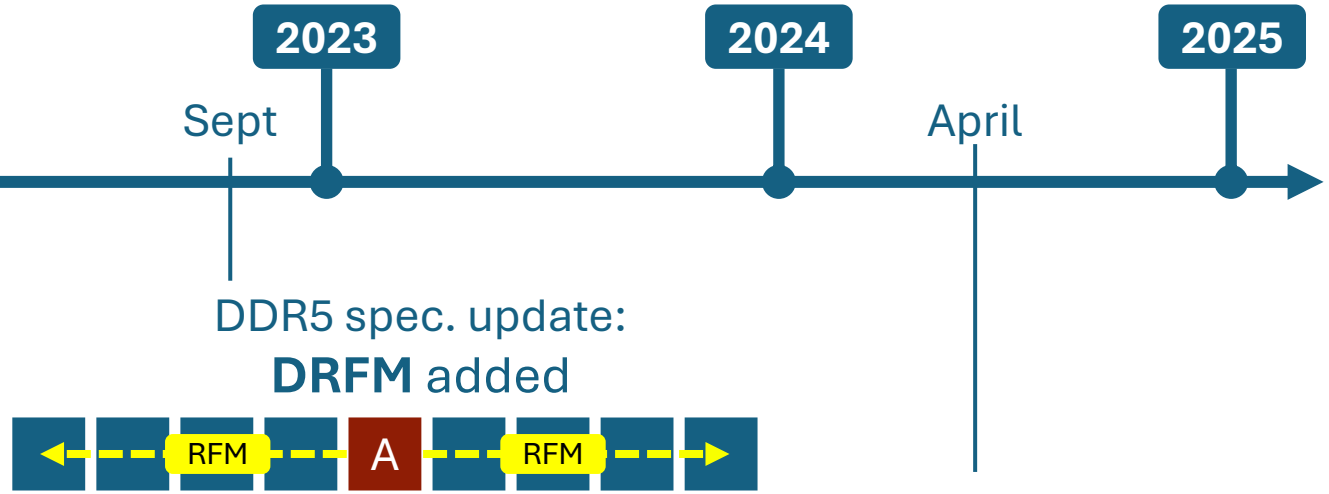

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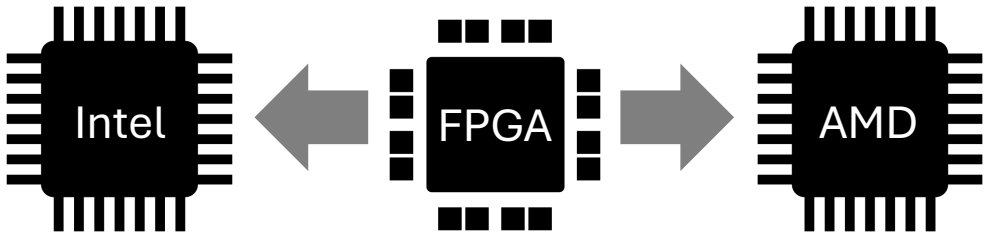
Rowhammer pattern execution



Conclusion

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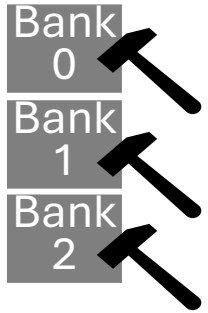

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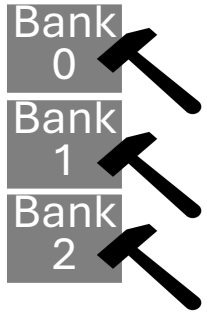

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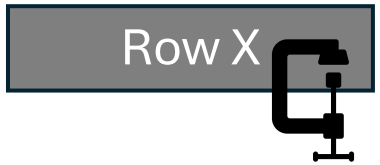

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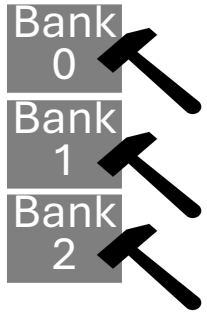

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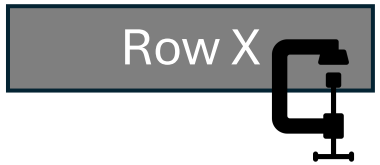

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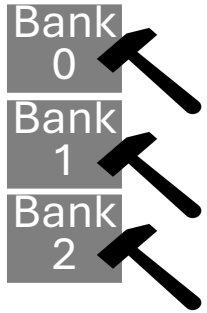

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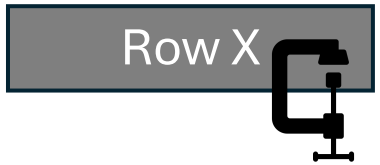

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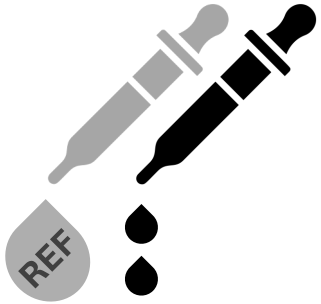

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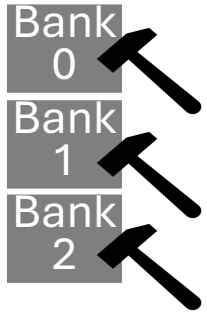

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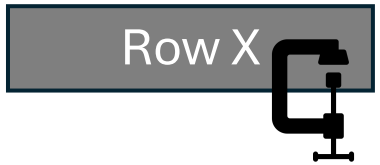

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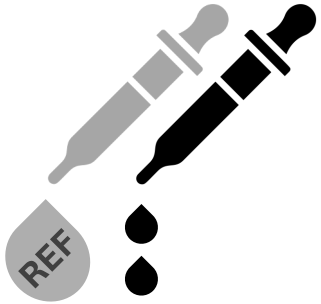

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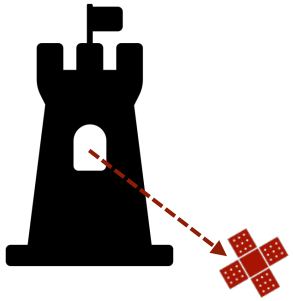

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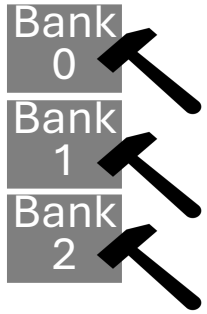
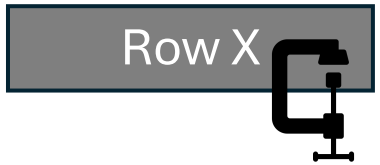
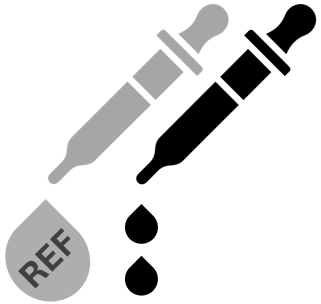
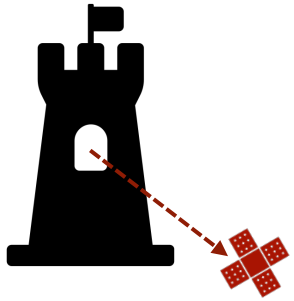
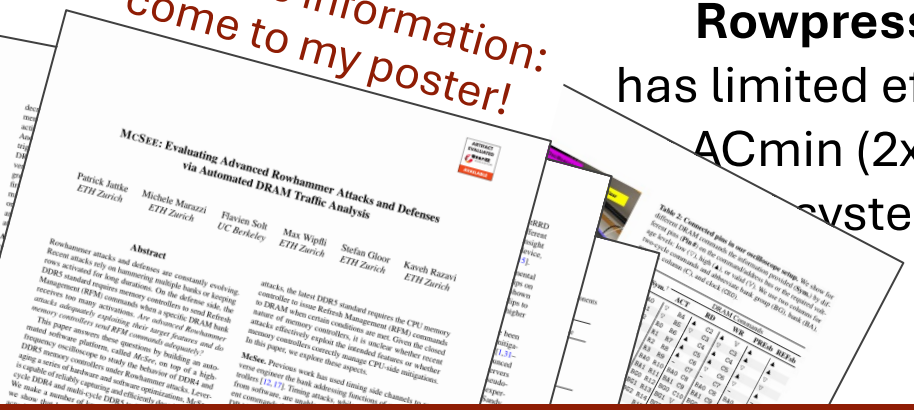








For more information: come to my poster!



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