Systematic Evaluation of Randomized Cache Designs against Cache Occupancy

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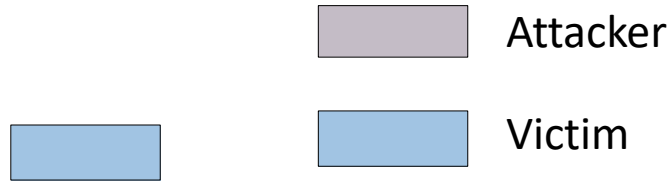
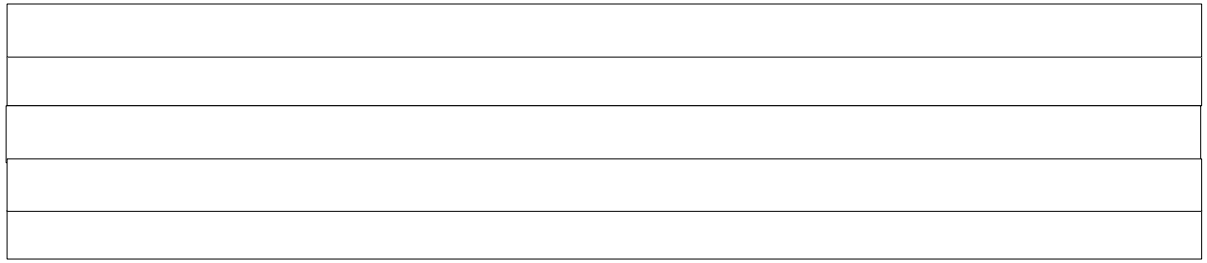
Prime+Probe Attack





Prime+Probe in a cache set

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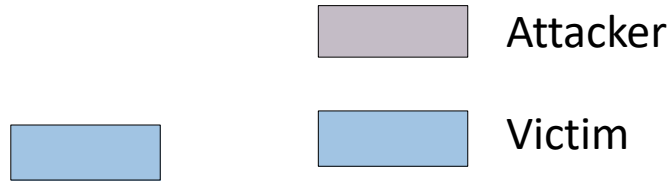

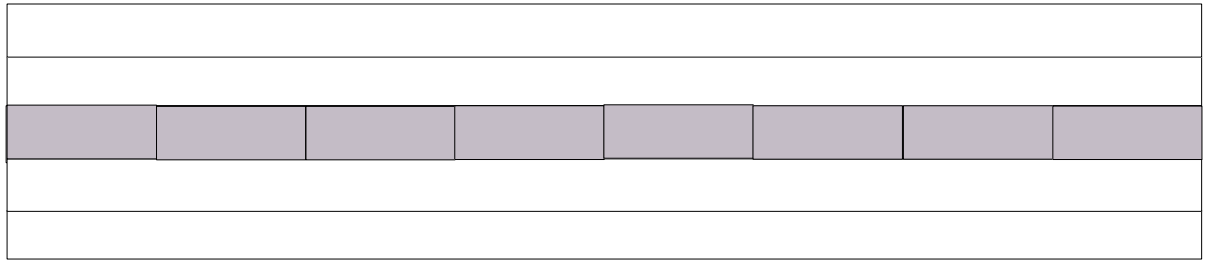

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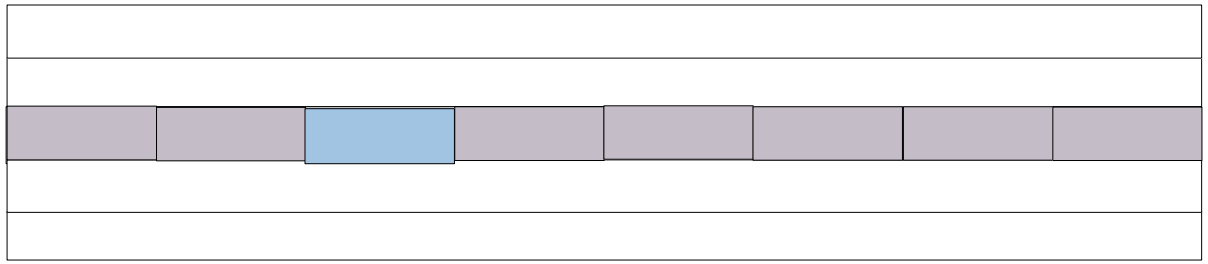

Attacker

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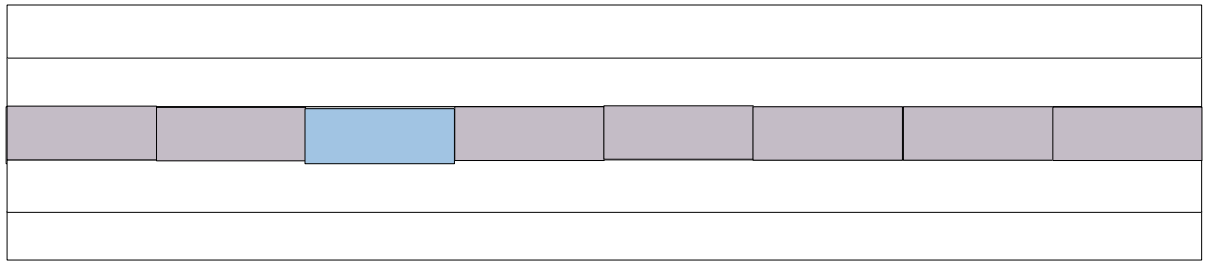

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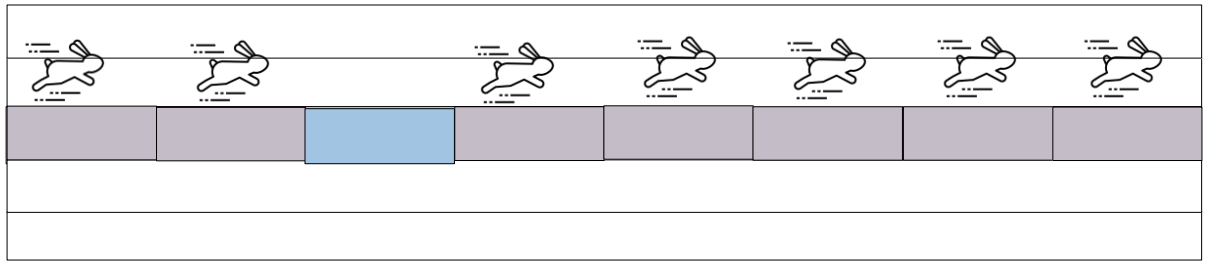

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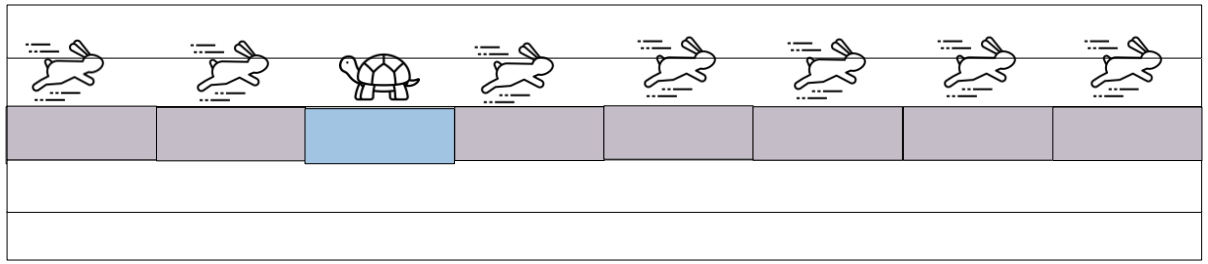

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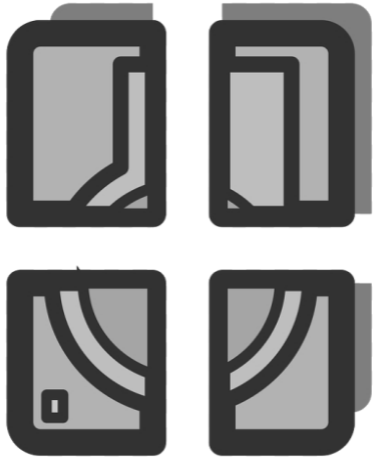
Randomized Caches

Randomization of addresses



Partitioning of Cache

Cache Occupancy Attacks

Occupancy Attack in entire cache

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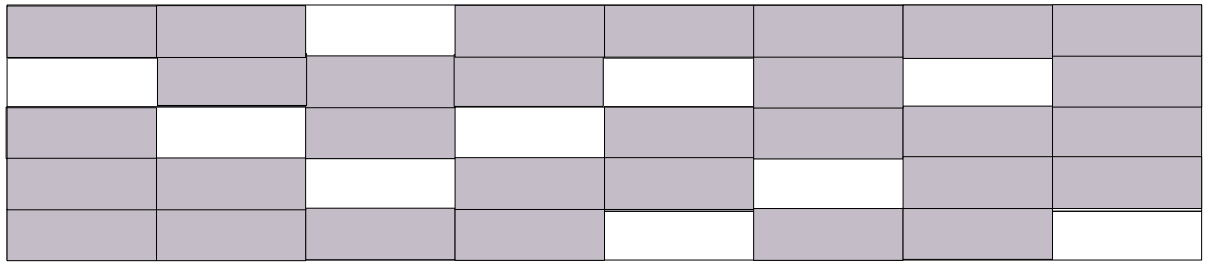
Cache Occupancy Attacks



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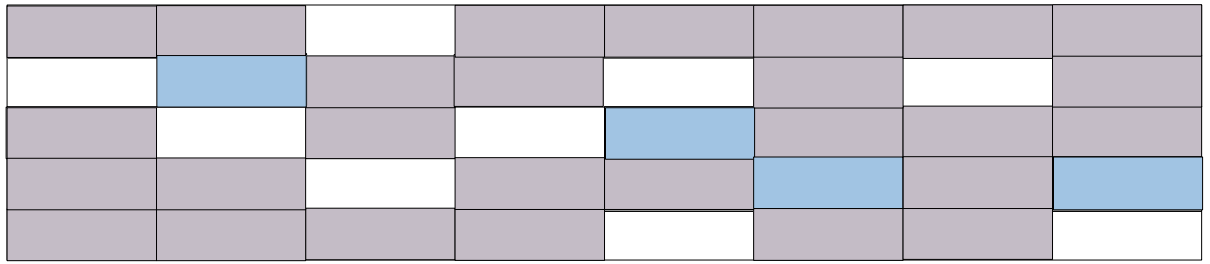

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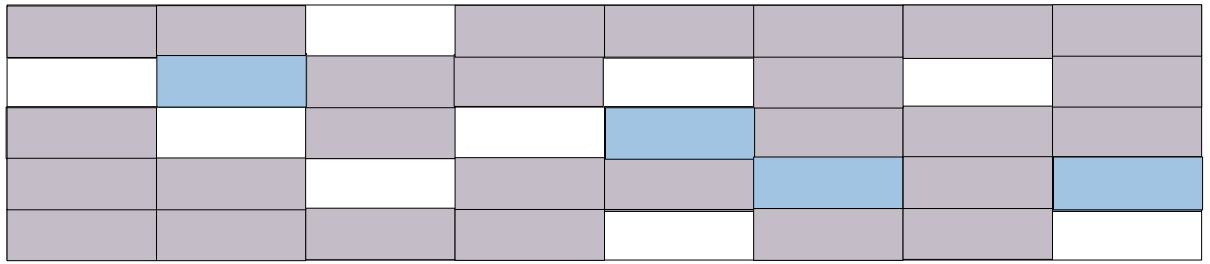

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Motivation

State of the Art

- **Randomized Caches** – obfuscate address to cache-set mapping
- **Multiple design principles** – constantly evolving field

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This Work

- **Performance Impact** – Evaluation across various replacement policies
- **Security Impact –** Testing resilience against cache occupancy attacks

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- Benchmarking *under spurious cache occupancy* that removes this implementation assumption of MIRAGE and provides a fair baseline for all cache design
- Evaluate the performance five different replacement policies - RandomRP, TreePLRURP, WeightedLRURP, RRIPRP, and FIFORP

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Comparative Performance Evaluation

- **Platform**: gem5
- **Workload**: Spurious occupancy followed by SPEC2017
- **LLC size**: 16 MB
- **Skews** (wherever applicable): 2

L1 size: L1d : 512 KB, L1i : 32 KB
CPU model: TimingSimpleCPU
LLC replacement policy: various
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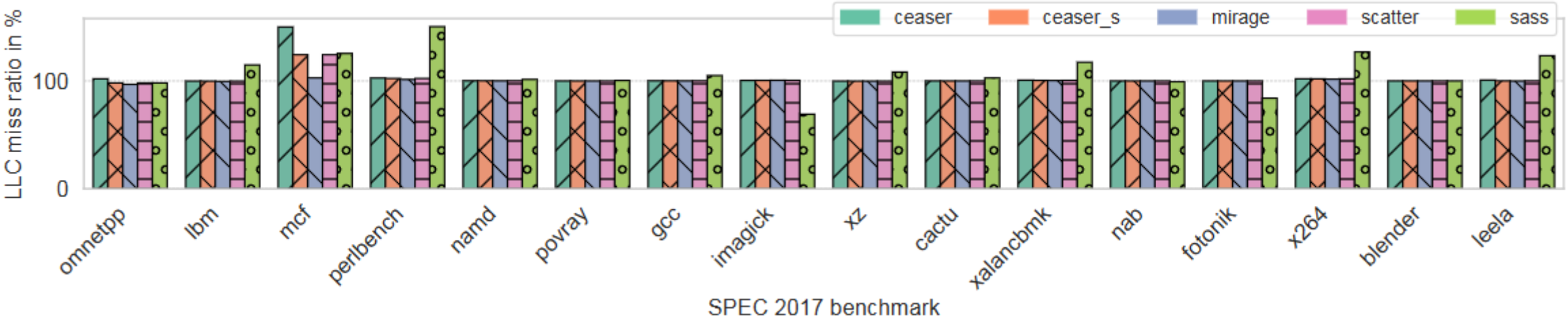
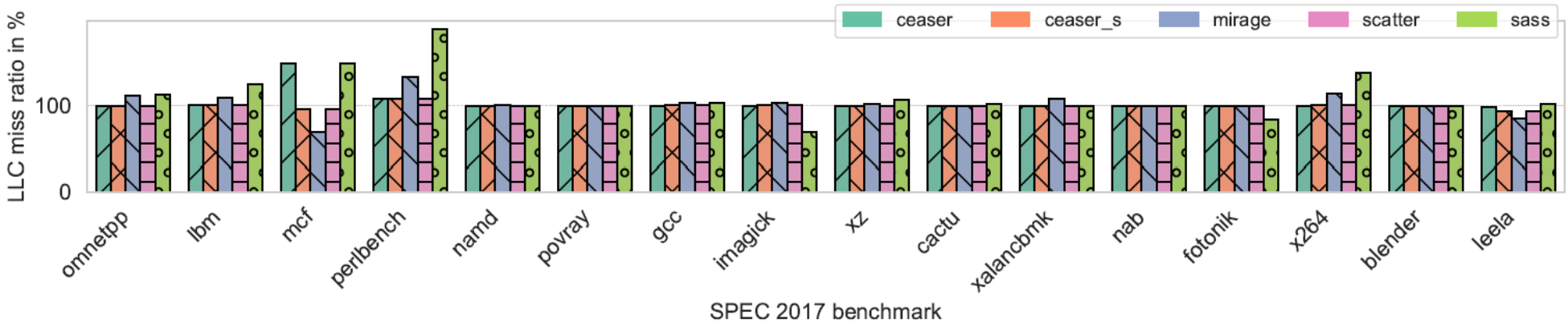


Performance evaluation of different cache designs with RandomRP replacement policy

Comparative Performance Evaluation



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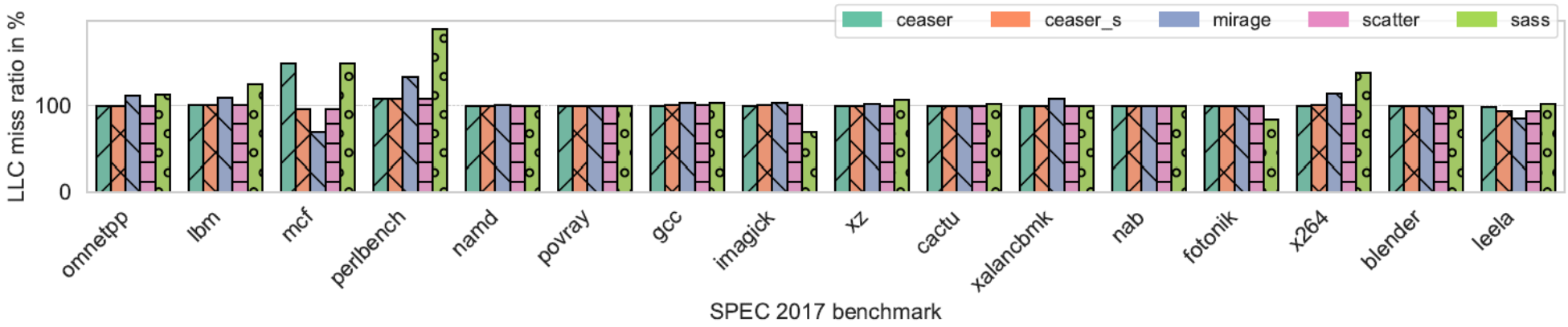

Performance evaluation of different cache designs with RRIPRP replacement policy

Takeaway

- While most prior works are evaluated mostly with random replacement, we show that different cache designs have varied effects of replacement policies
- For some replacement policies, certain randomized cache designs actually outperform baseline set-associative cache

Cache Occupancy Attack: covert channel

Receiver

Sender

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① Allocates sufficient memory space and randomly accesses ℓ number of addresses.

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Cache Occupancy Attack: covert channel

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① Allocates sufficient memory space and randomly accesses ℓ number of addresses.

③ Re-accesses all the ℓ addresses it has previously installed in the cache.

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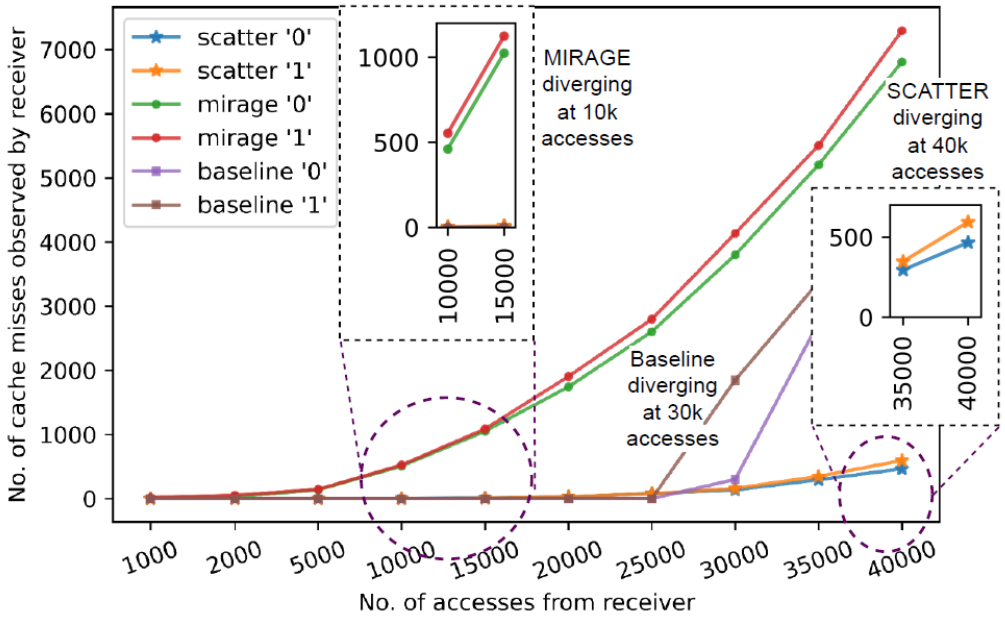
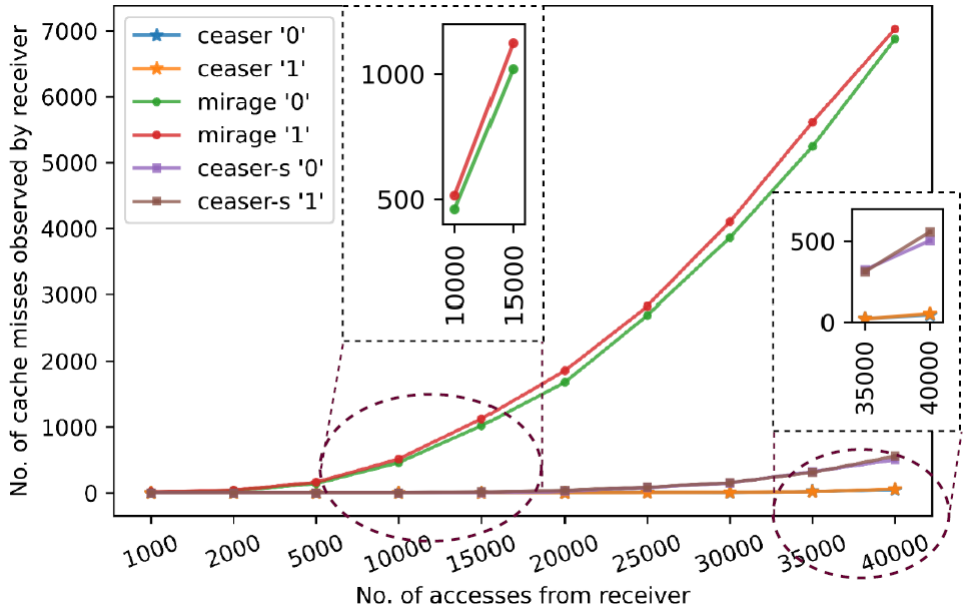


Cache occupancy channel in MIRAGE, ScatterCache and baseline set-associative cache



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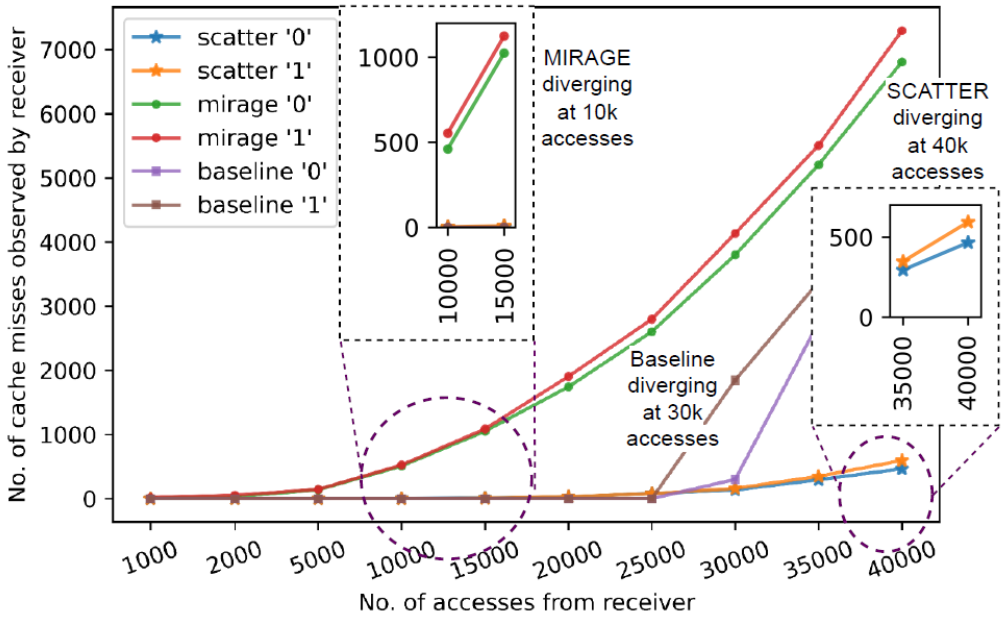

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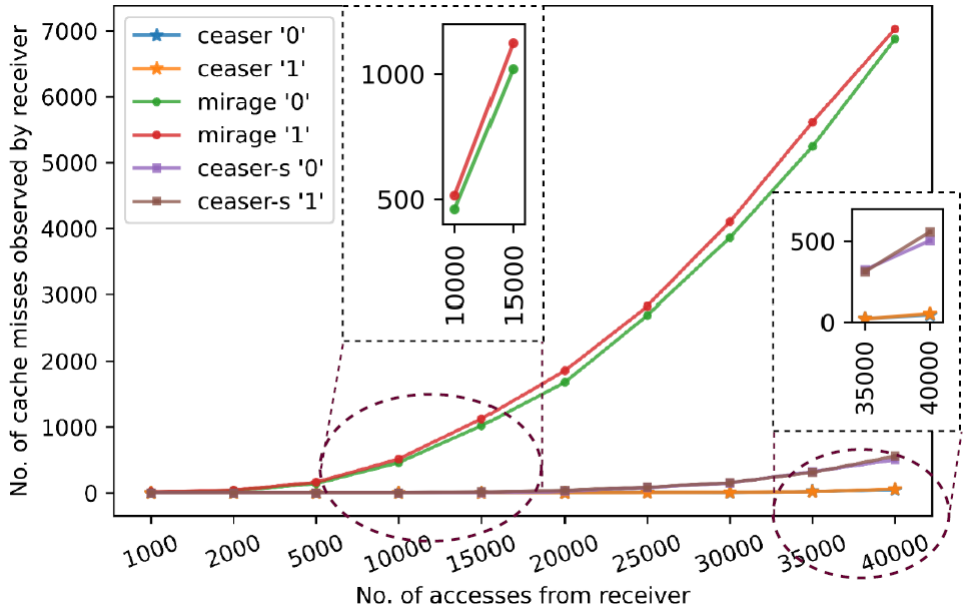
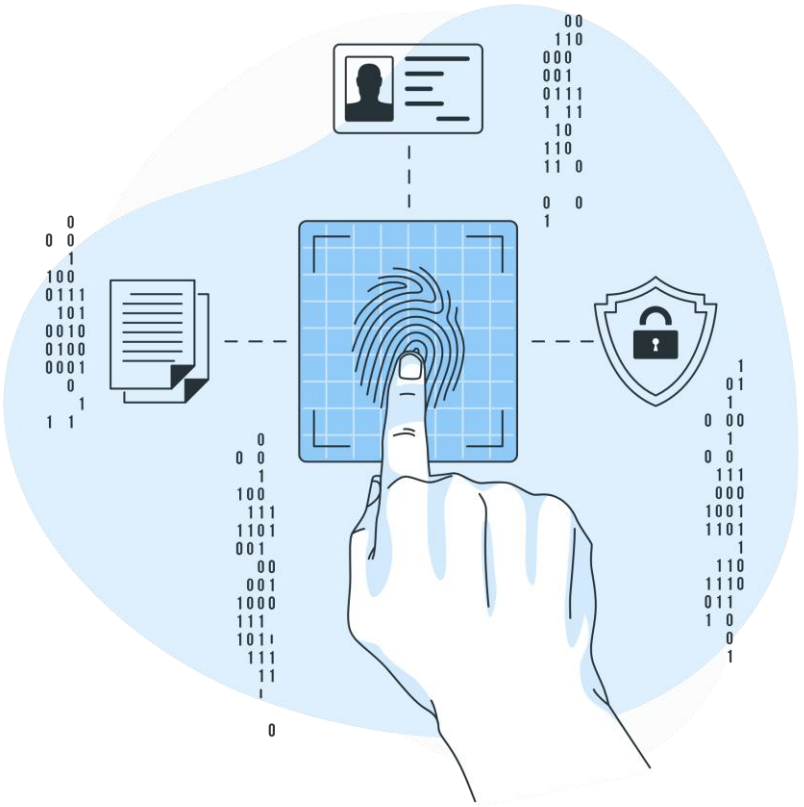


Cache occupancy channel in MIRAGE, CEASER and CEASER-S cache designs

Takeaway

MIRAGE, due to its policy of compulsory eviction from the data store for every new address installation, is more vulnerable to cache occupancy attacks than other designs, including baseline set-associative cache.



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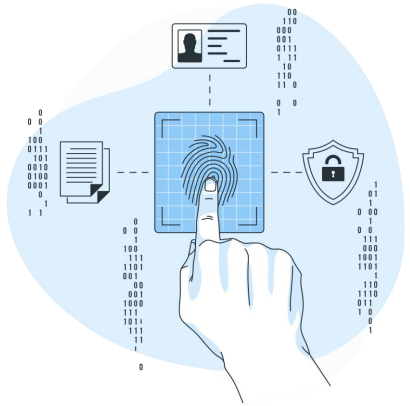

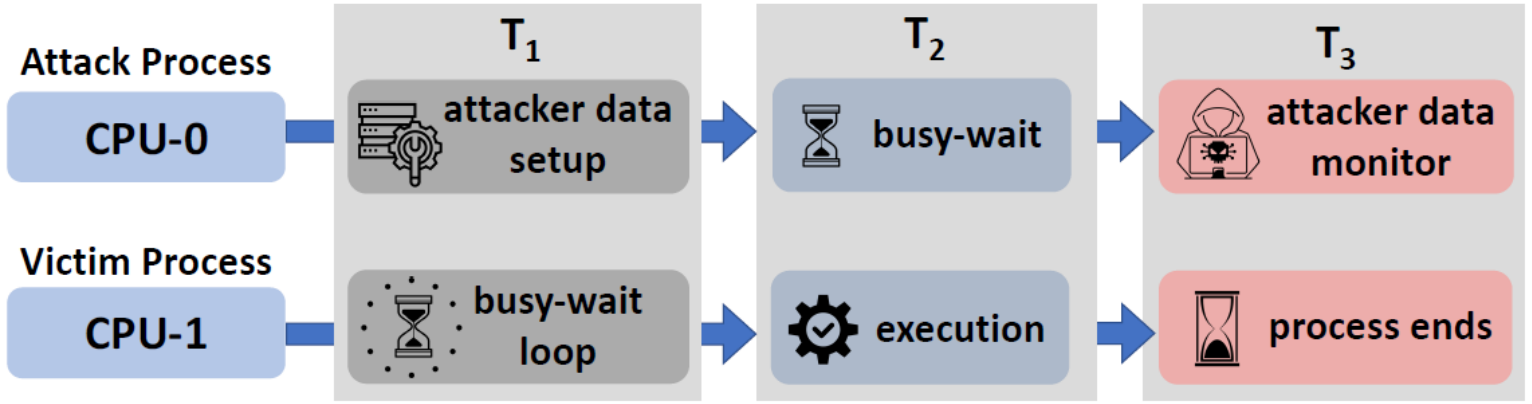

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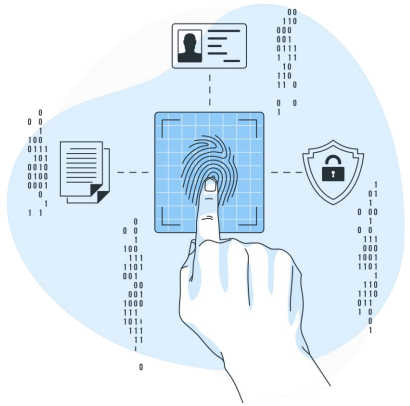

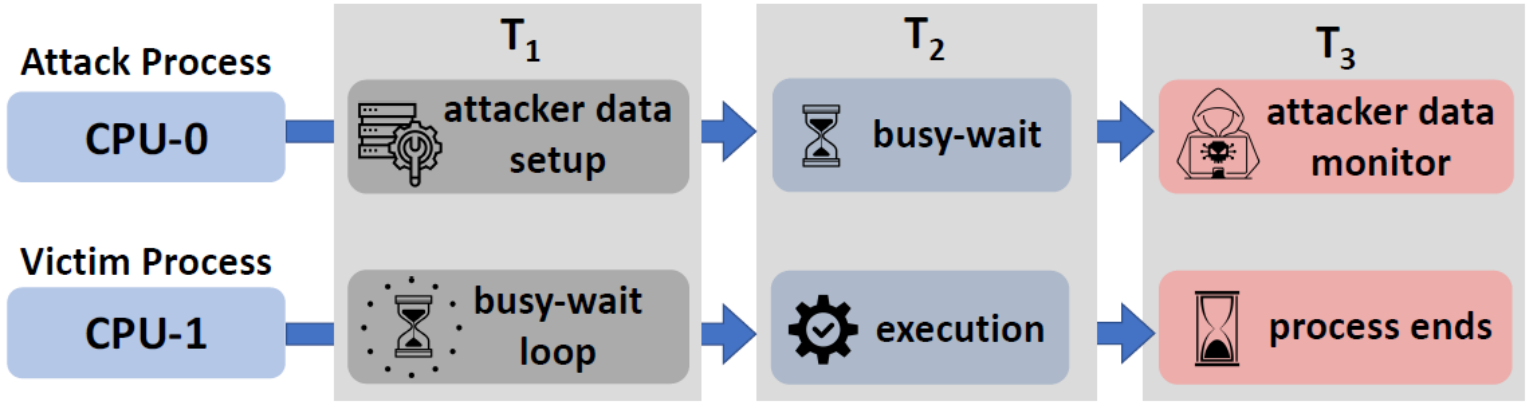

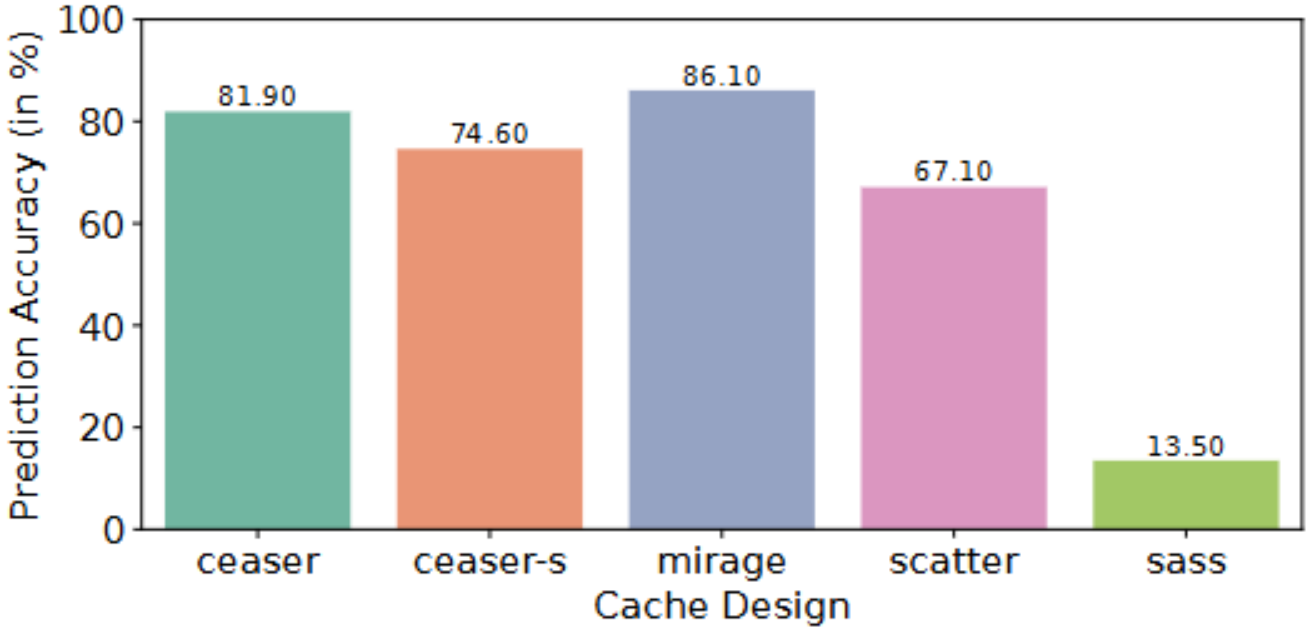

Fingerprinting accuracy across different cache designs of SPEC2017 workloads.

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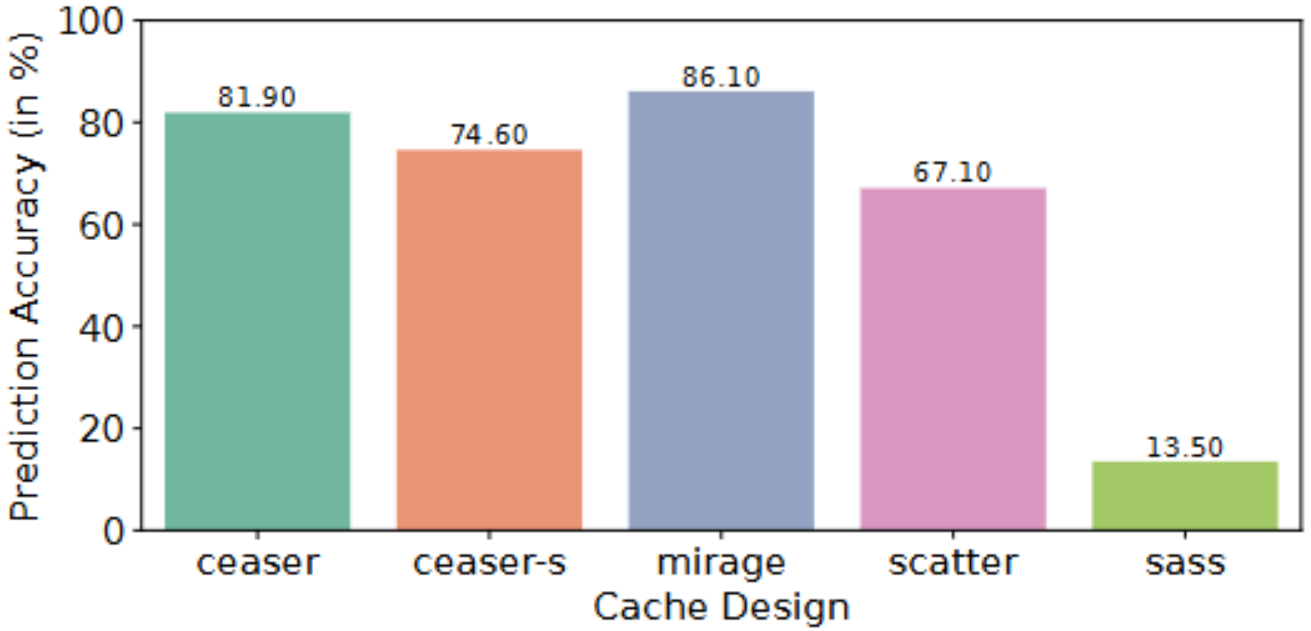

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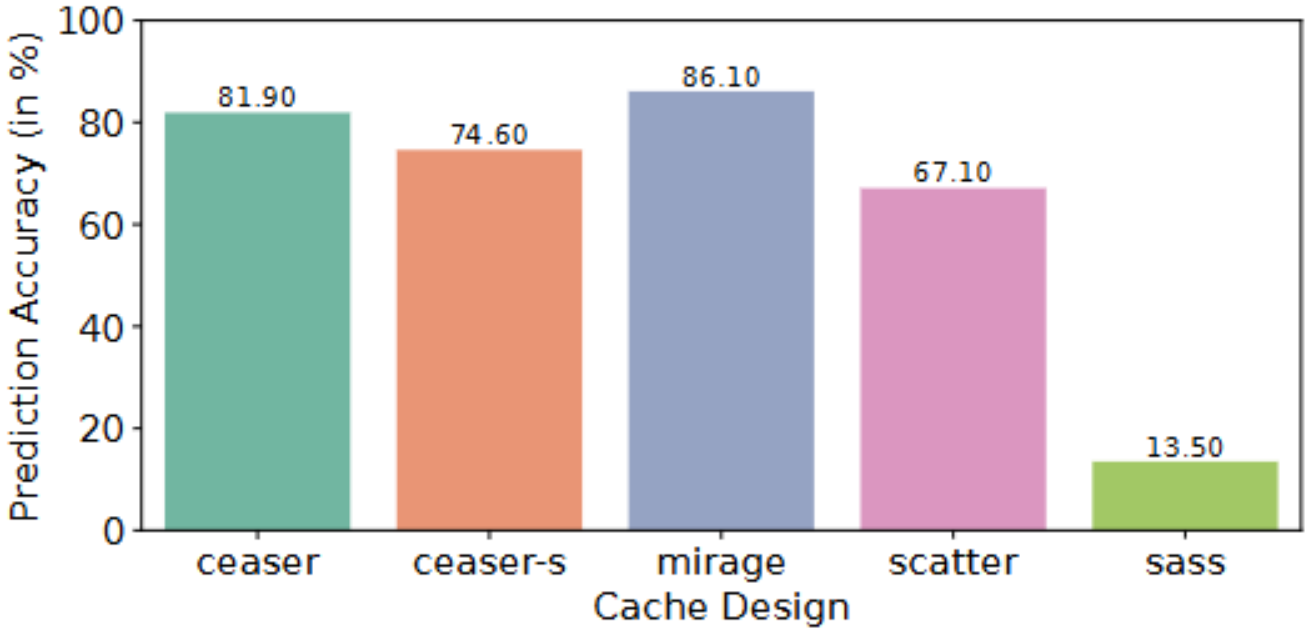

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- SassCache exhibits a remarkably less prediction accuracy, implying no statistically significant adversarial advantage wrt. process fingerprinting.

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5. A single observation point for the attacker is the tuple (P, C, T): the time T taken to access its own cache occupancy after the AES victim operates upon plaintext P for an unknown key K

Cache Occupancy Attack: AES key recovery

Total number of templates created by the adversary $= 256 \times 16$

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Creates templates of access time T_j^* for each byte of known key K^* for last round attack

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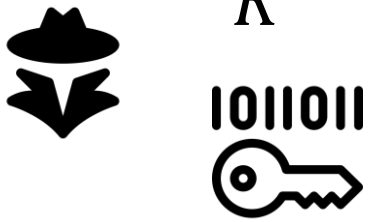

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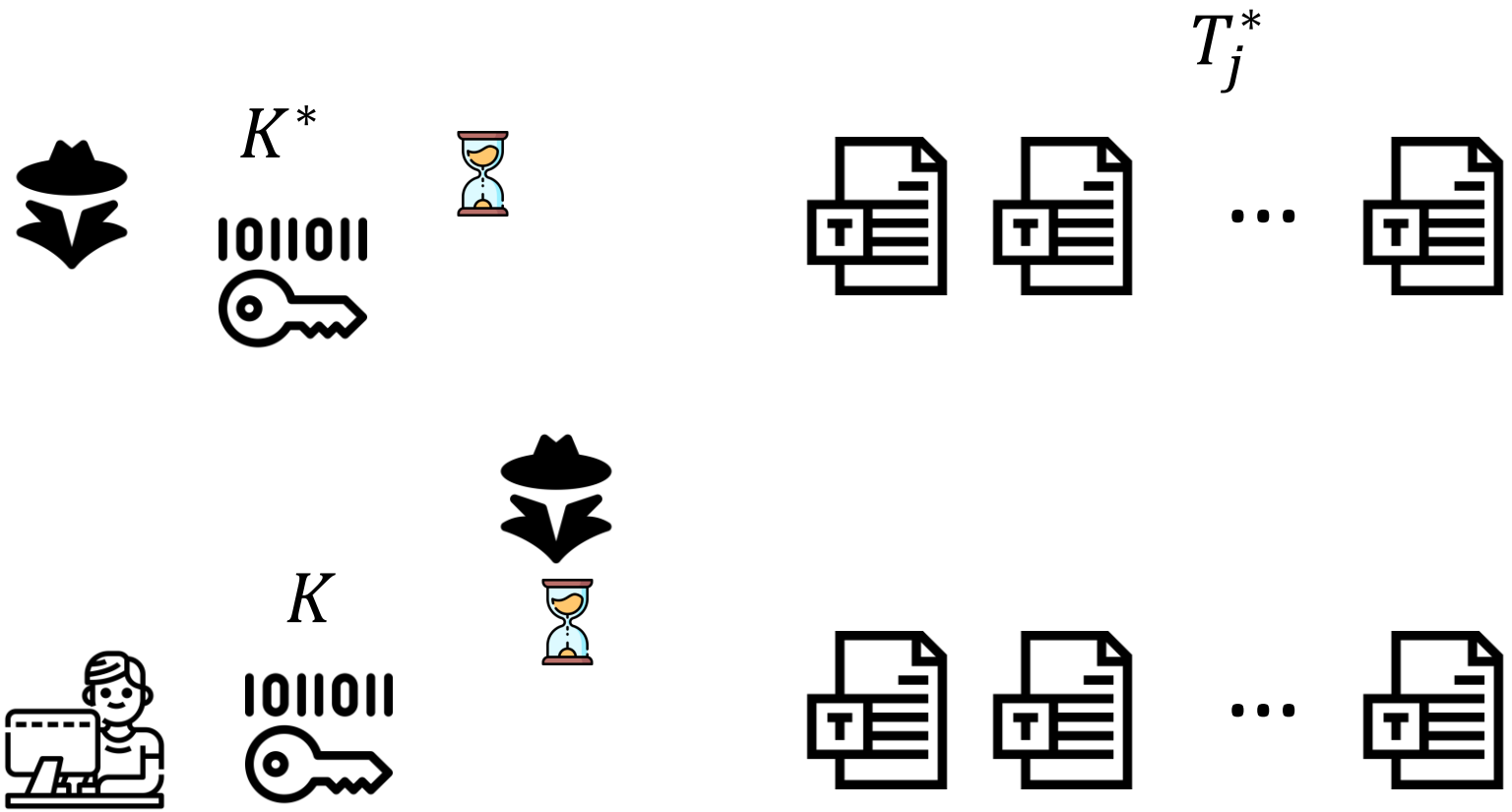

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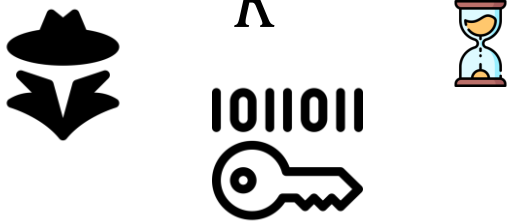

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- Lower GE implies the key bytes are lower ranked post correlation, thereby enabling faster key recovery

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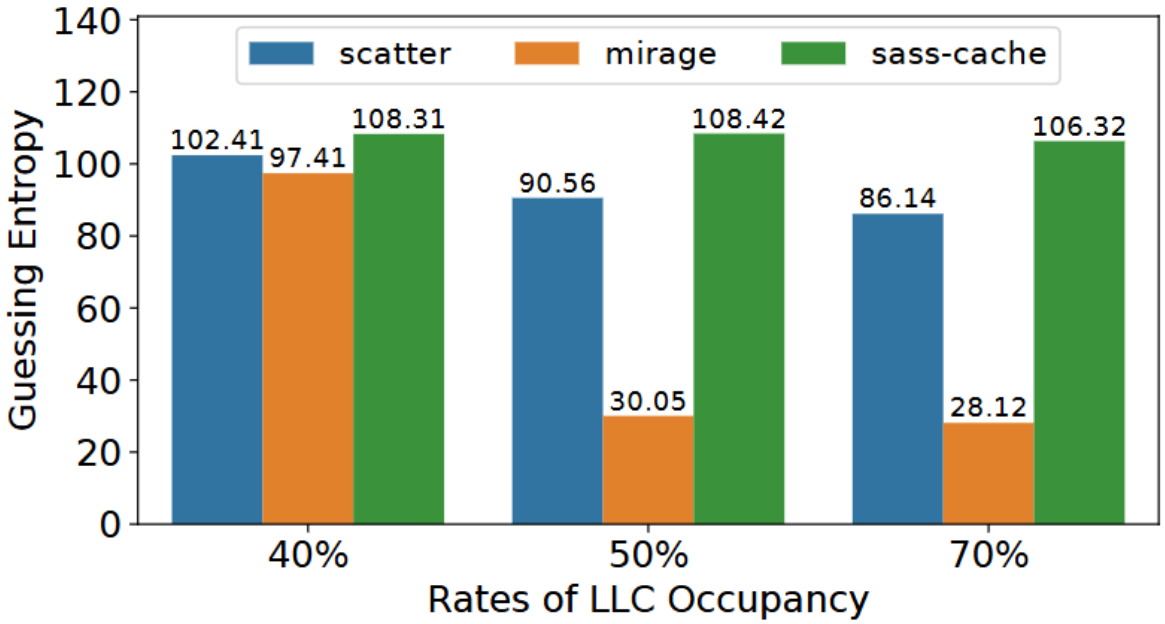

Key Recovery experiment across three occupancy rates: 40%, 50%, 70%

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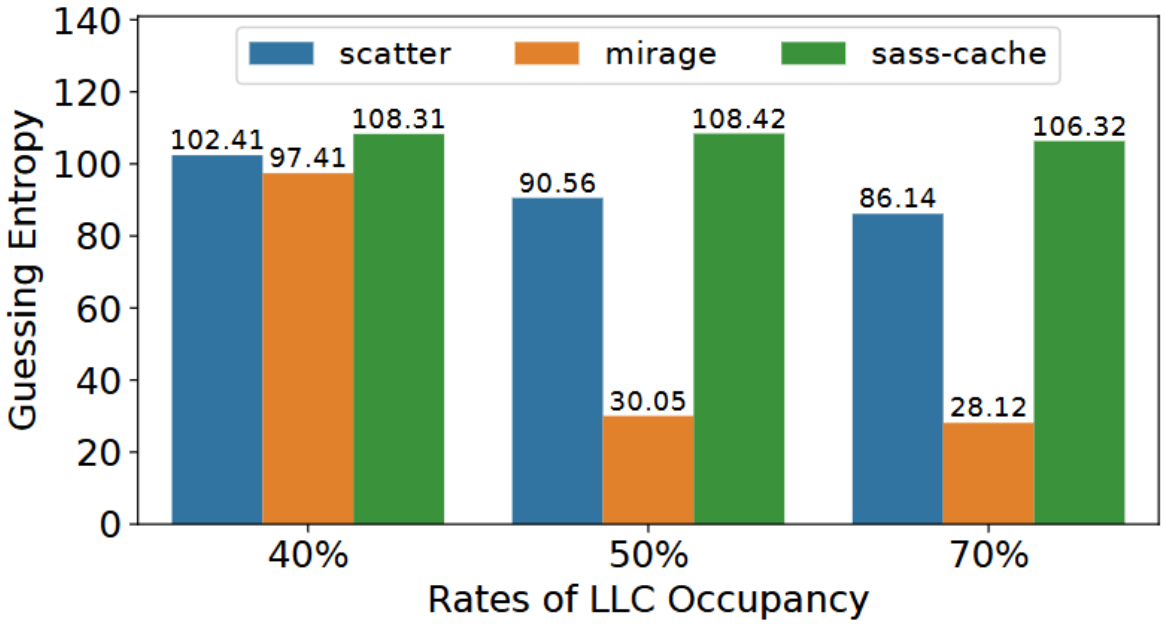

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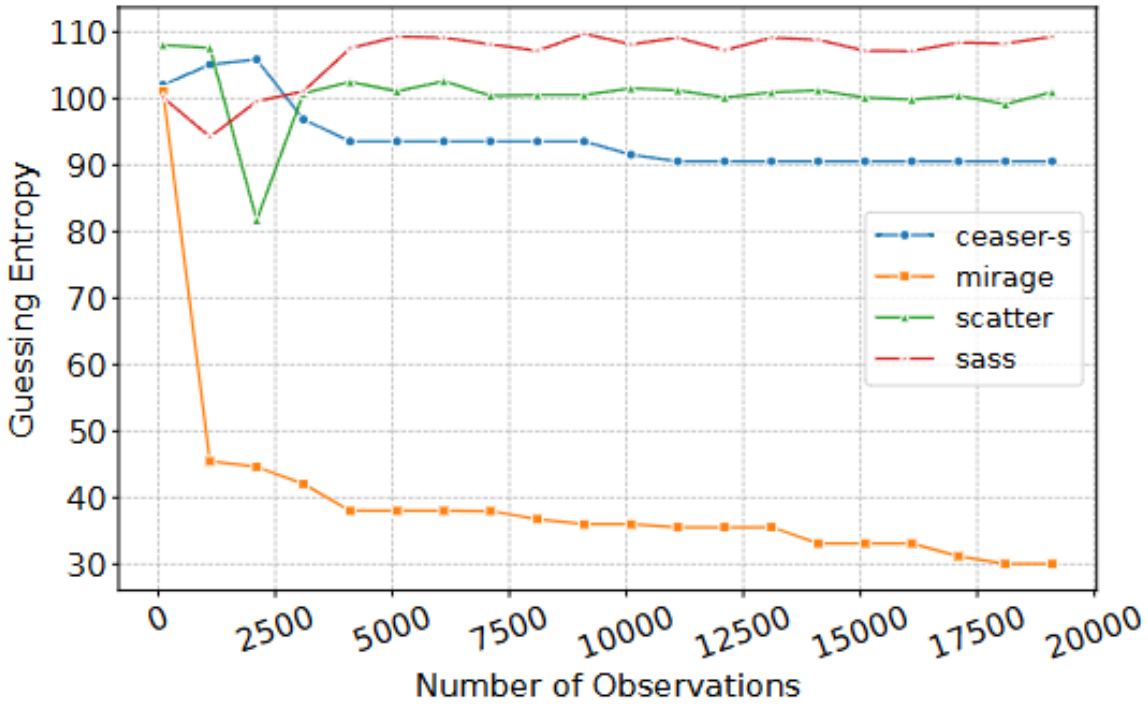
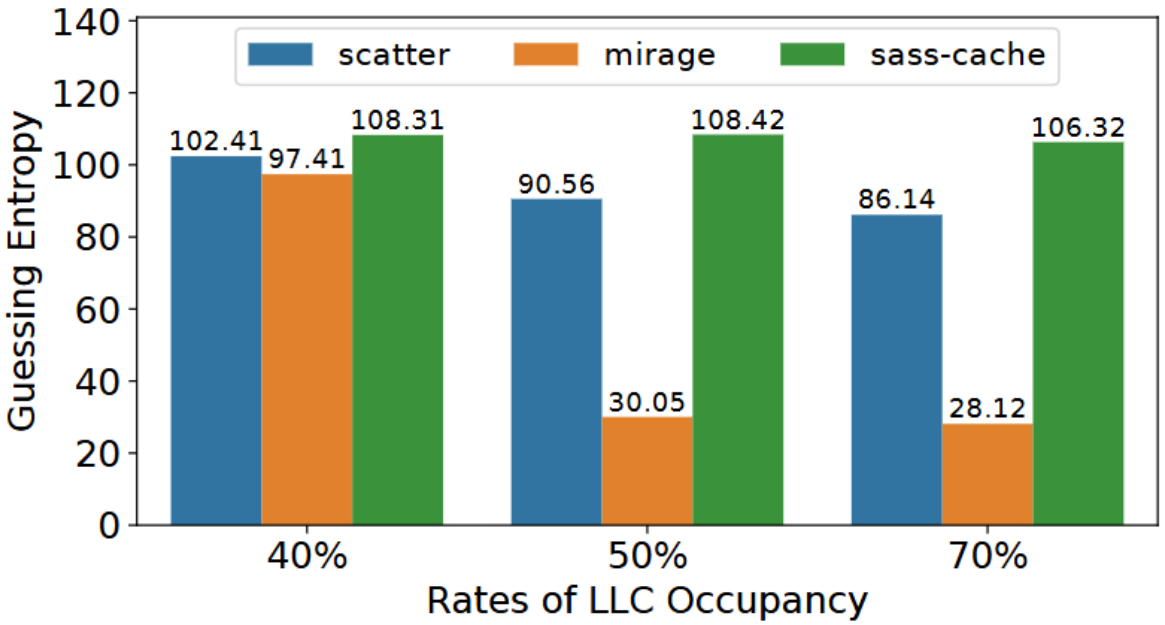
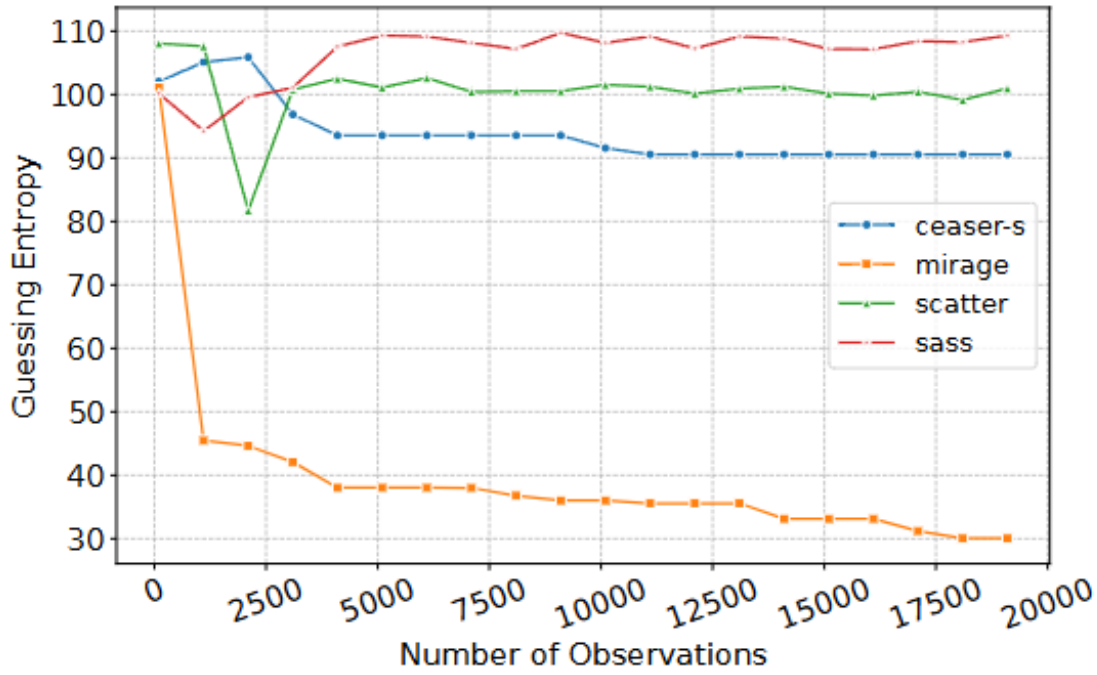


Key Recovery experiment across a fixed occupancy rate: 50%

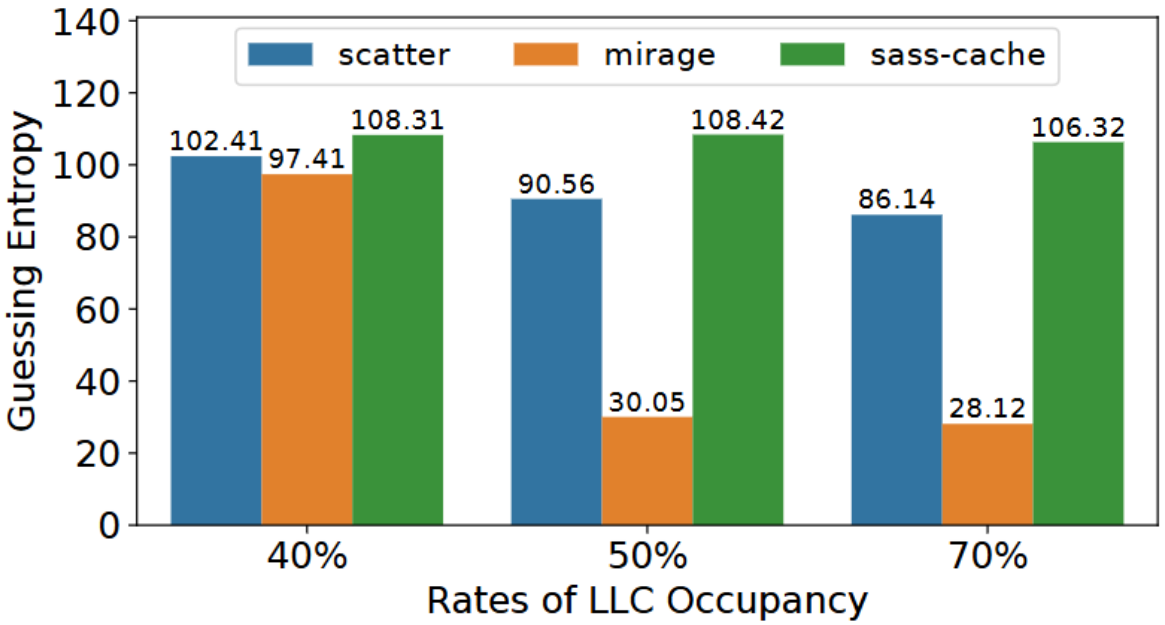
Cache Occupancy Attack: AES key recovery

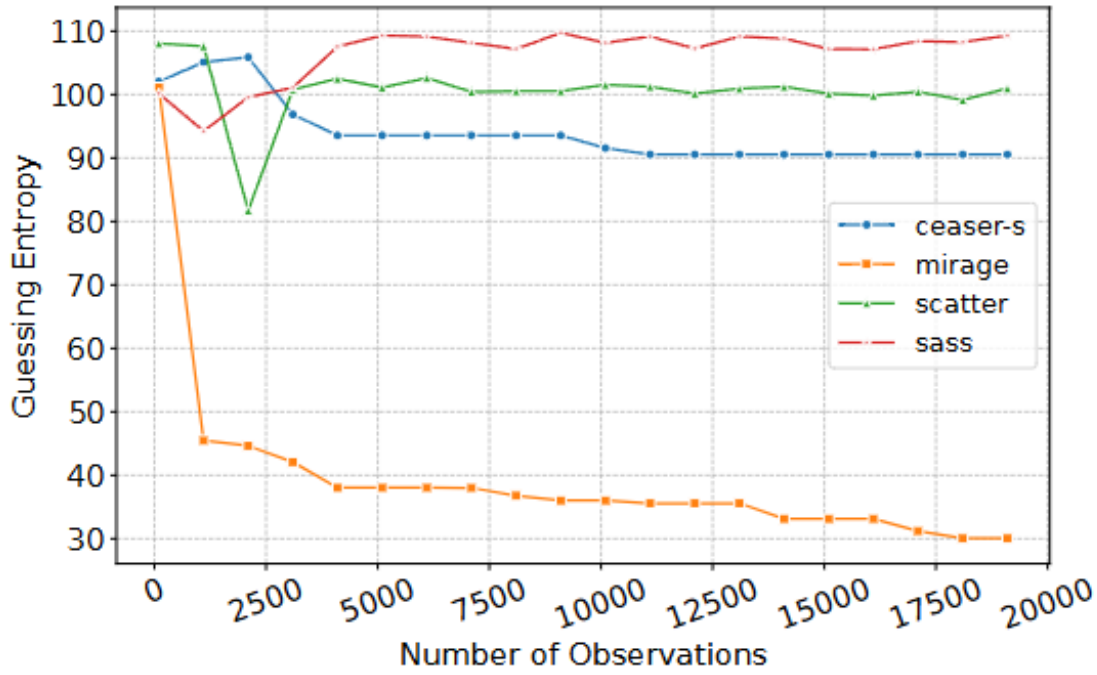




Takeaway

Cache Occupancy Attack: AES key recovery





Takeaway

Designs based on set-associative caches are more resilient to cache occupancy attacks compared to designs based on pseudo-fully associative caches.

Summary

- **Performance and security analysis** of randomized cache designs across multiple replacement policies and Cache Occupancy attacks.
- **First Key recovery** attacks on T-table based **AES-128** using different occupancy levels and guessing entropy
- Establishes Cache Occupancy attack as a **serious concern** like contention attacks for secured cache designs.

Summary

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Thank you for your attention!