

Rage Against the Machine Clear: A Systematic Analysis of Machine Clears and Their Implications for Transient Execution Attacks

Hany Ragab*, Enrico Barberis*, Herbert Bos and Cristiano Giuffrida

*Equal contribution joint first authors



Vrije Universiteit Amsterdam

Speculative Execution

```
if (x < array_size) {  
    y = array[x]  
}
```

Data cache



Not cached

Speculative Execution

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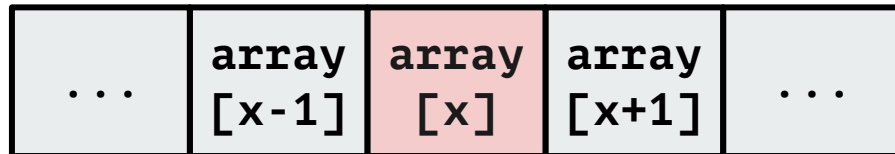


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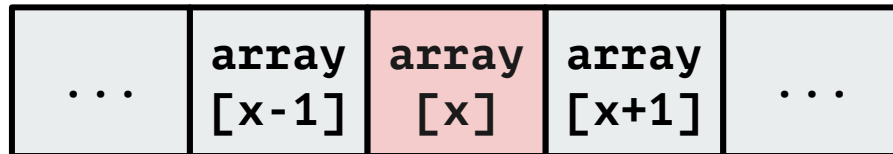


- Cached
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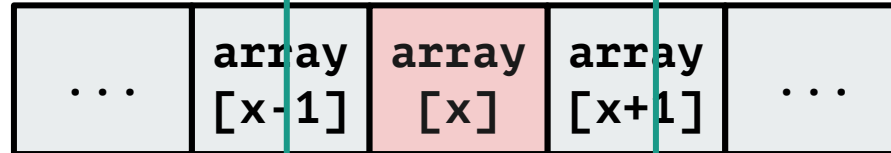


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Speculative Execution

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Data cache



■ Cached
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Bad Speculation



The root cause of discarding issued μ Ops on x86 processors

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Branch Misprediction

Bad Speculation



The root cause of discarding issued μ Ops on x86 processors

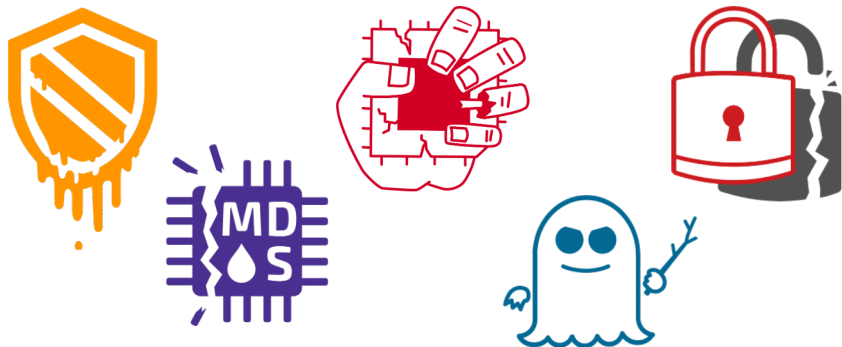
Branch Misprediction

Machine Clear

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Branch Misprediction & Intel TSX

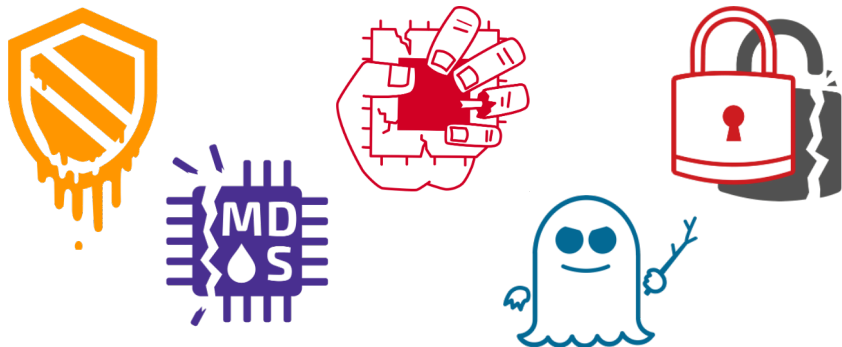


Machine Clear

Bad Speculation

The root cause of discarding issued μ Ops on x86 processors

Branch Misprediction & Intel TSX



Machine Clear



Rage Against The Machine Clear



**Self-Modifying Code
Machine Clear**

**Floating-Point
Machine Clear**

**Memory Ordering
Machine Clear**

**Memory Disambiguation
Machine Clear**

Rage Against The Machine Clear



**Self-Modifying Code
Machine Clear**

**Floating-Point
Machine Clear**



Rage Against The Machine Clear



**Self-Modifying Code
Machine Clear**



**Speculative Code
Store Bypass
(SCSB)**

Negligible mitigation
overhead

**Floating-Point
Machine Clear**

Rage Against The Machine Clear



**Self-Modifying Code
Machine Clear**



**Speculative Code
Store Bypass
(SCSB)**

Negligible mitigation
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**Floating-Point
Machine Clear**



**Floating-Point
Value Injection
(FPVI)**

53% Mitigation
overhead

Rage Against The Machine Clear



Self-Modifying Code
Machine Clear

Floating-Point
Machine Clear



End-to-end exploit
leaking arbitrary
memory in Firefox

With a leakage rate
of **13 KB/s**

Security Analysis of Machine Clear



Security Analysis of Machine Clear



1. Architectural Invariant

Security Analysis of Machine Clear



1. Architectural Invariant
2. Invariant Violation

Security Analysis of Machine Clear



1. Architectural Invariant
2. Invariant Violation
3. Security Implications

Security Analysis of Machine Clear



1. Architectural Invariant
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4. Exploitation

Self-Modifying Code Machine Clear



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Self-Modifying Code is a program storing instructions as data, modifying its own code as it is being executed

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i1: ...

i2: store nop @ i3

i3: load secret

i4: ...

i5: ...

Self-Modifying Code Machine Clear

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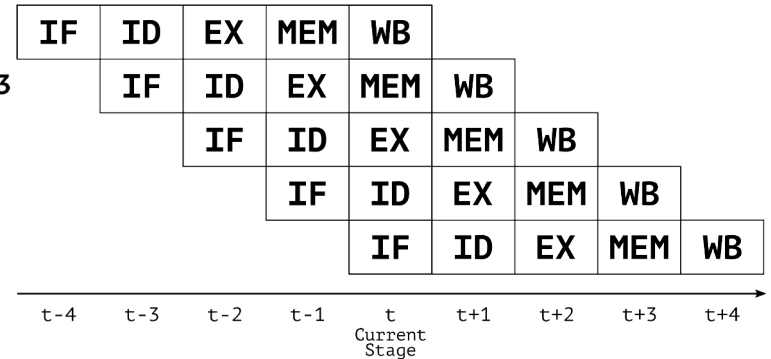
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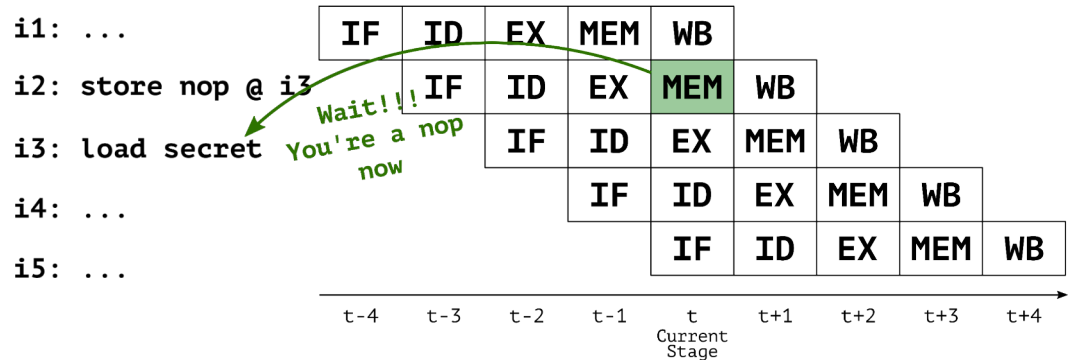
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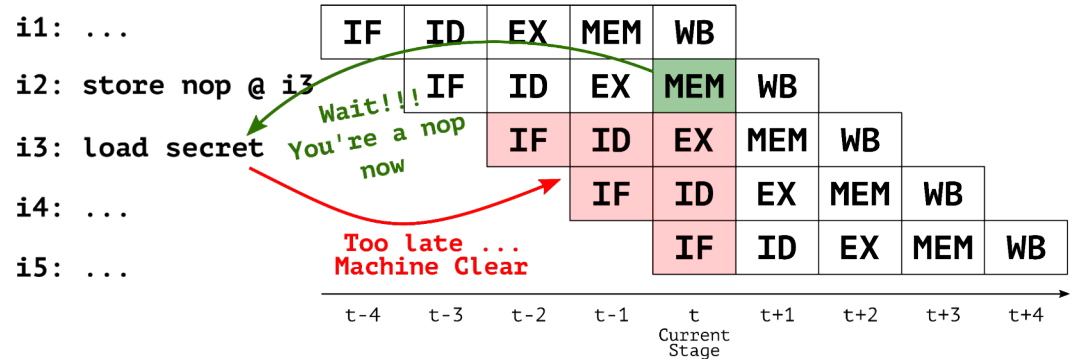
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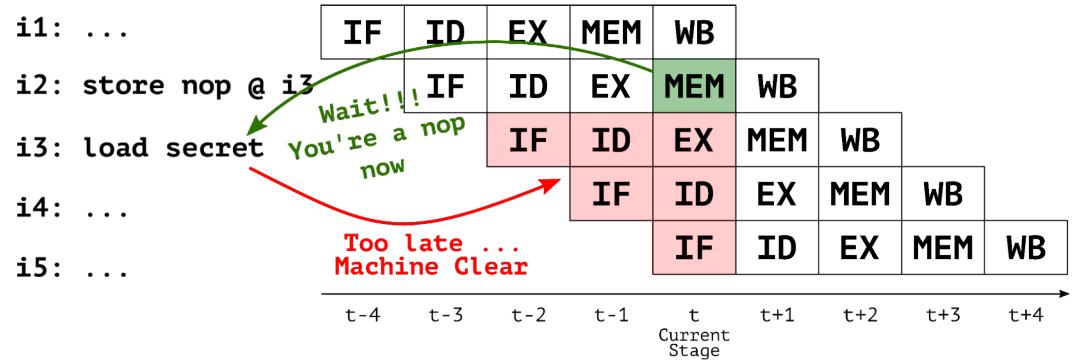


- SMC Detection
- Transiently Done

Self-Modifying Code Machine Clear

Self-Modifying Code is a program storing instructions as data, modifying its own code as it is being executed

Architectural Invariant
Stores always target data



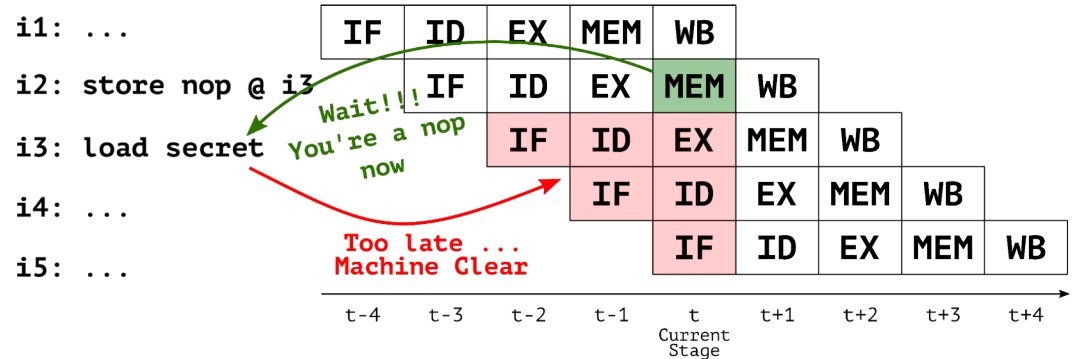
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Invariant Violation
Self-Modifying Code



■ SMC Detection
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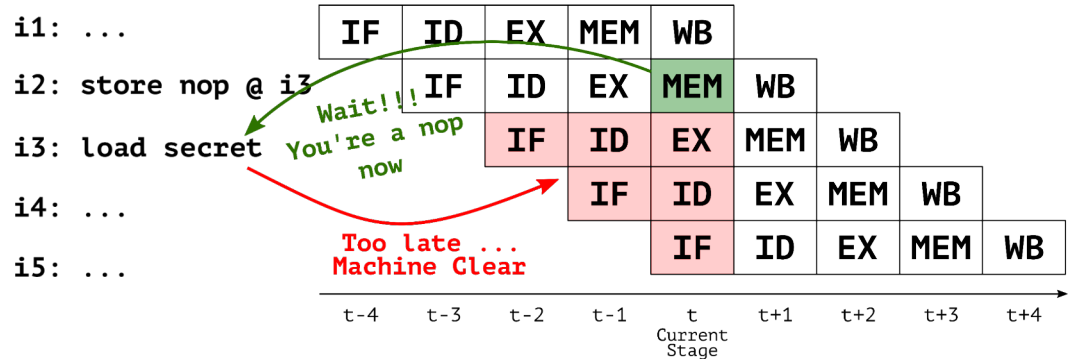
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Invariant Violation
Self-Modifying Code

Security Implications
Transiently execute stale code



■ SMC Detection
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Self-Modifying Code Machine Clear

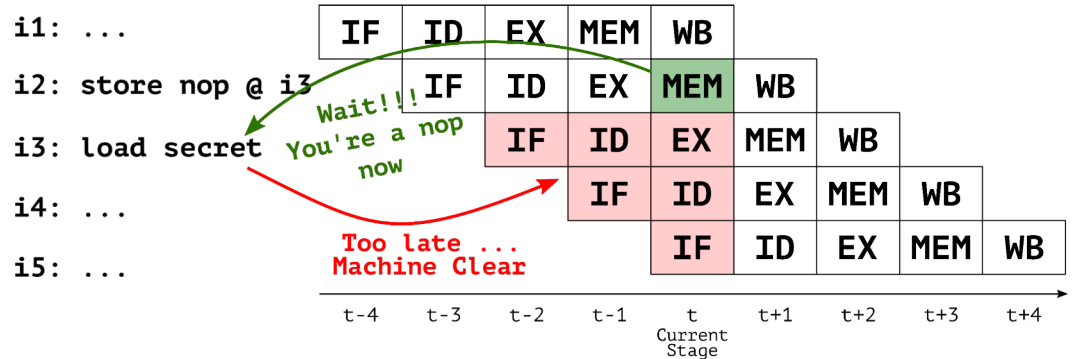
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?

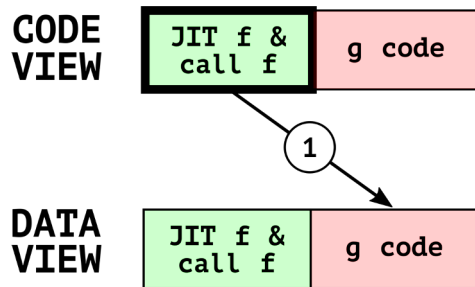


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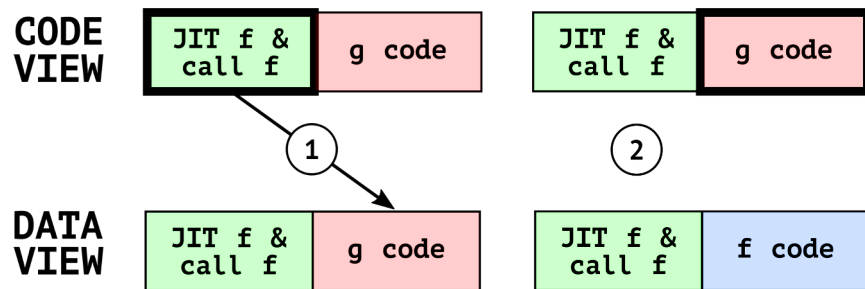
Speculative Code Store Bypass (SCSB)



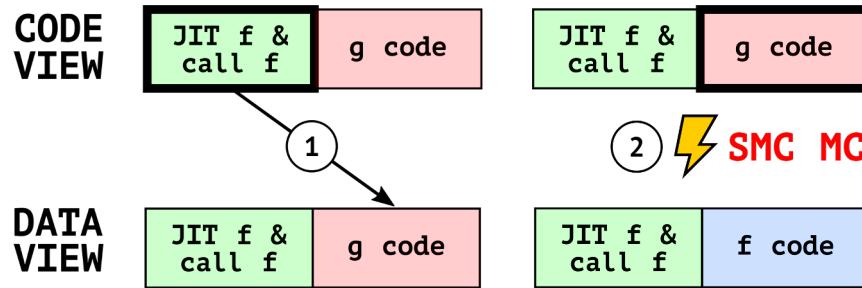
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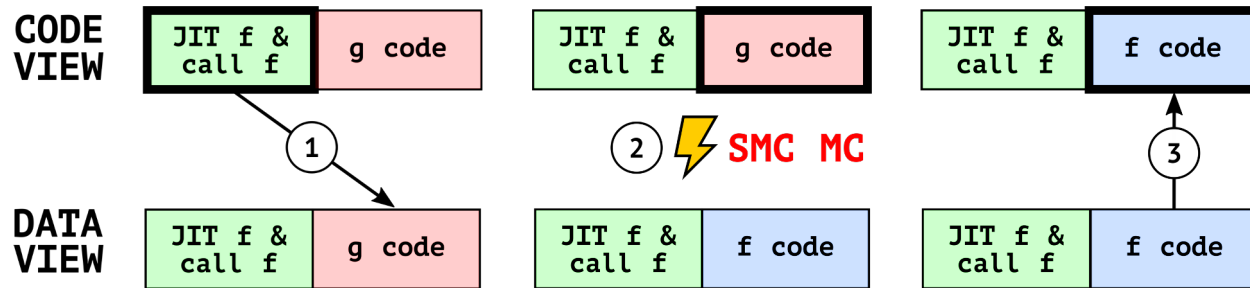
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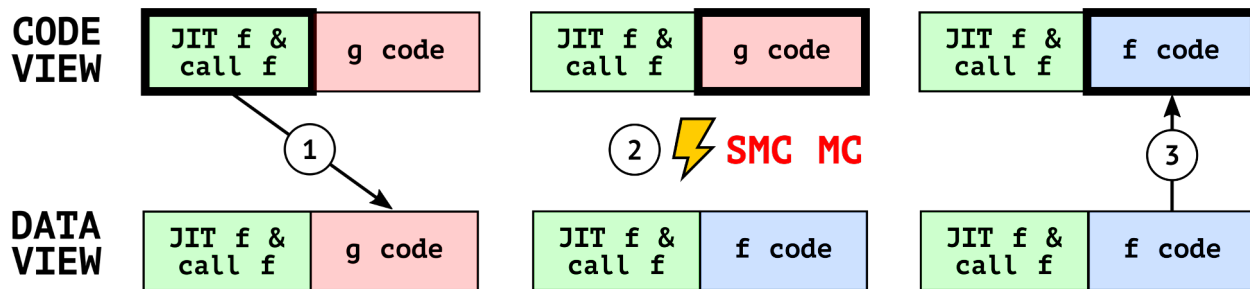
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8.1.3 Handling Self- and Cross-Modifying Code

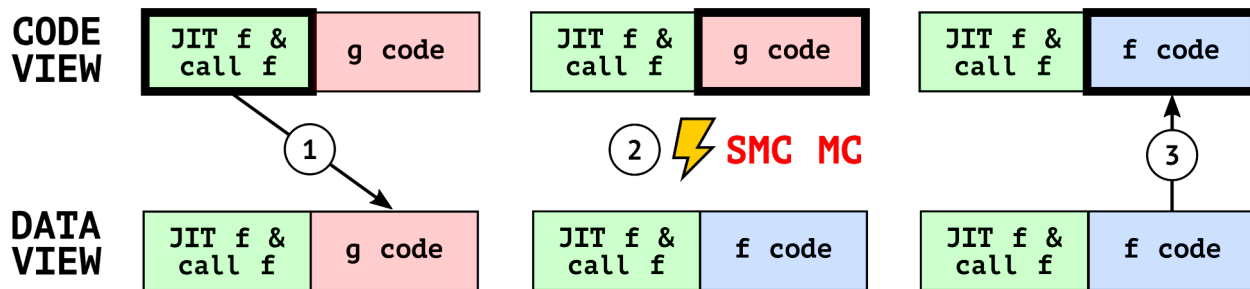
(* OPTION 1 *)

Store modified code (as data) into code segment;
Jump to new code or an intermediate location;
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Speculative Code Store Bypass (SCSB)



8.1.3 Handling Self- and Cross-Modifying Code

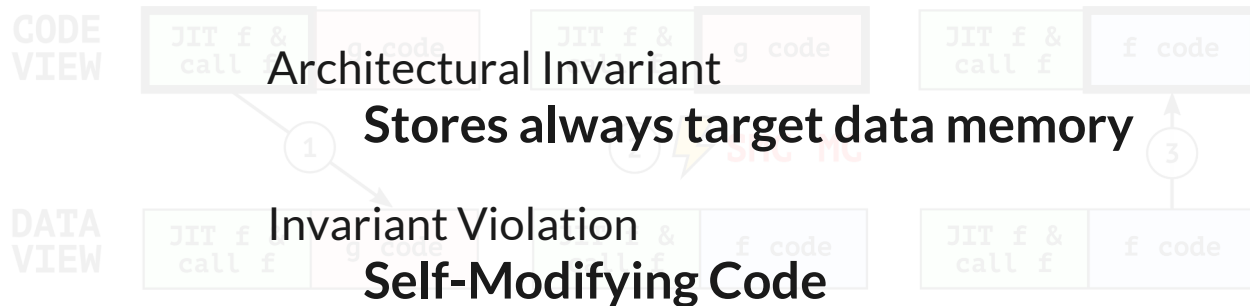
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8.1.3 Handling Self- and Cross-Modifying Code

Security Implications

Transiently execute stale code

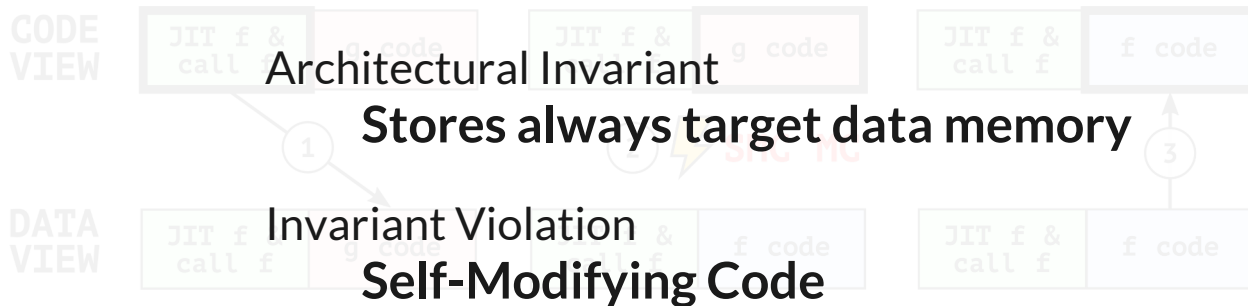
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Floating-Point Machine Clear



Subnormal/Denormal numbers are a special range of floating-point numbers with a value smaller than the smallest Normal number (i.e. 2^{-1022})

Floating-Point Machine Clear



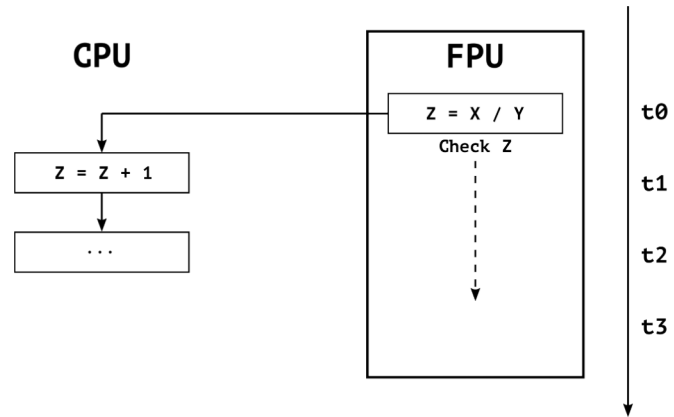
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i1: Z = X / Y  
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i3: ...
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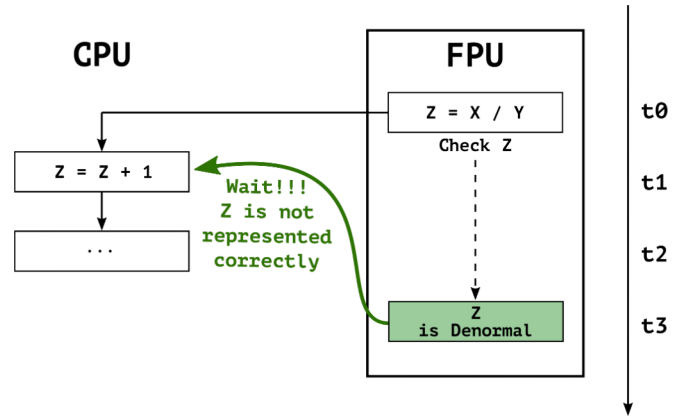
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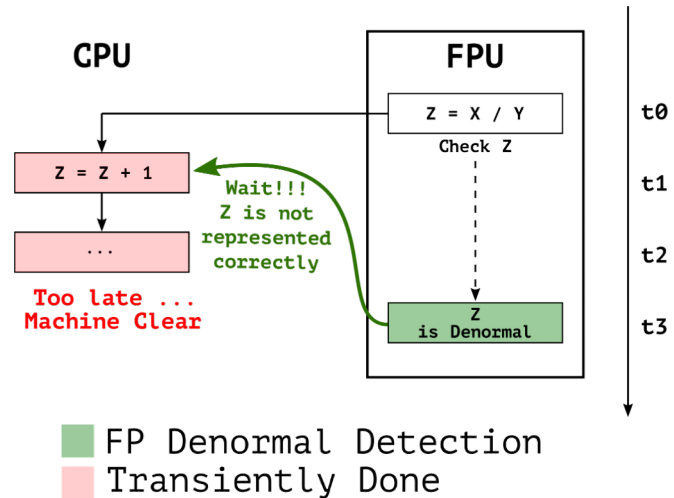
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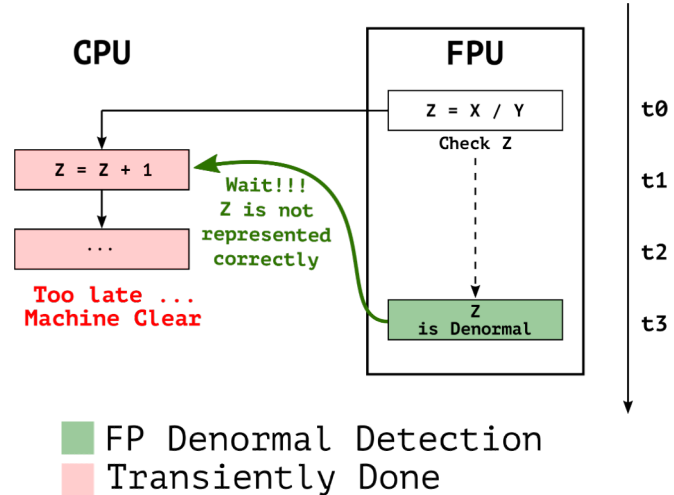


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Architectural Invariant
FPU always operates on normal numbers

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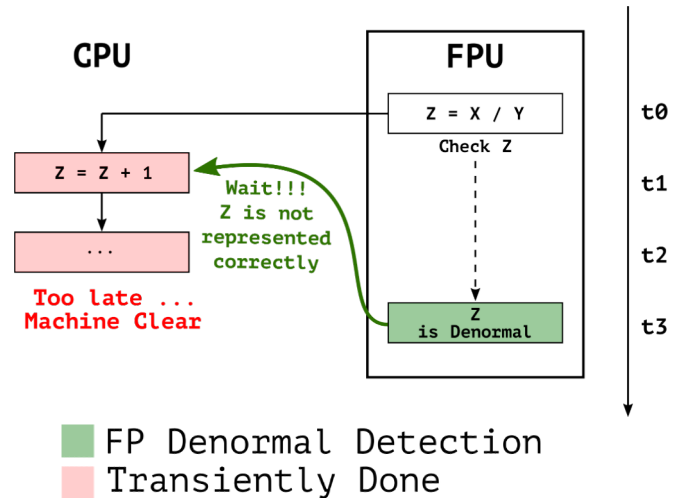
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Invariant Violation
Subnormal FP operations

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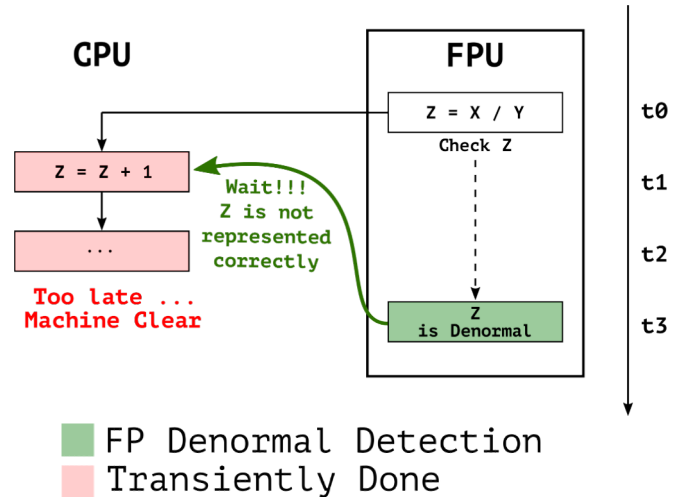
Invariant Violation

Subnormal FP operations

Security Implications

Transiently inject arbitrary FP values

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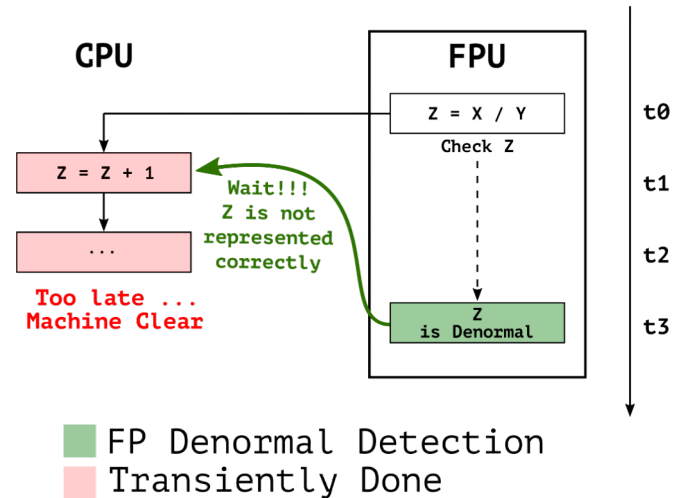
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Exploitation

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Floating-Point Value Injection (FPVI)



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0xffb0deadbeef000  
JSVAL_TYPE_STRING  
PAYLOAD:  
0xdeadbeef000
```

Floating-Point Value Injection (FPVI)

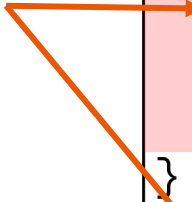
```
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//x = 0xc000e8b2c9755600  
//y = 0x0004000000000000  
z = x/y  
if (typeof z === "string") {
```

Floating-Point Value Injection (FPVI)

<code>0xfffb0deadbeef000</code> JSVAL_TYPE_STRING PAYLOAD: <code>0xdeadbeef000</code>	<code>0xff00000000000000</code> JSVAL_TYPE_DOUBLE PAYLOAD: <code>-Infinity</code>
--	--

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if (typeof z === "string") {  
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} else {  
    return z //z=-Infinity  
}
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//x = 0xc000e8b2c9755600
//y = 0x0004000000000000
z = x/y
if (typeof z === "string") {
  //z = 0xffffb0deadbeef000
  //leak byte @ 0xdeadbeef004
  return buf[(z.length&0xff)<<10]
} else {
  return z //z=-Infinity
}
```

Floating-Point Value Injection (FPVI)

Architectural Invariant

FPU always operates on normal numbers

Invariant Violation

Denormal FP operations

Security Implications

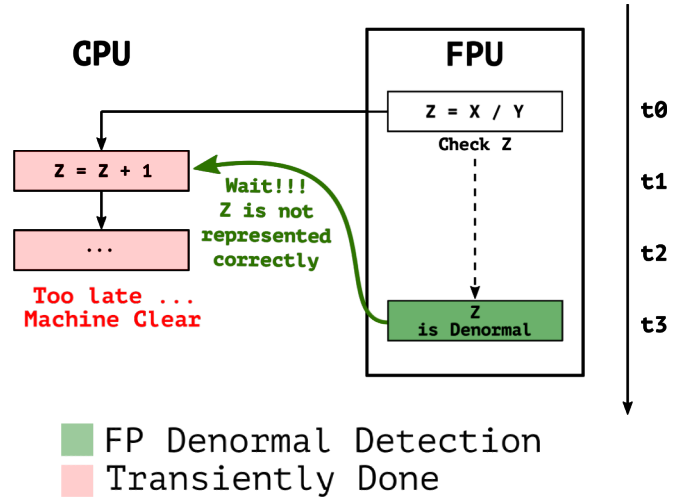
Transiently inject arbitrary FP values

Exploitation

Floating-Point Value Injection

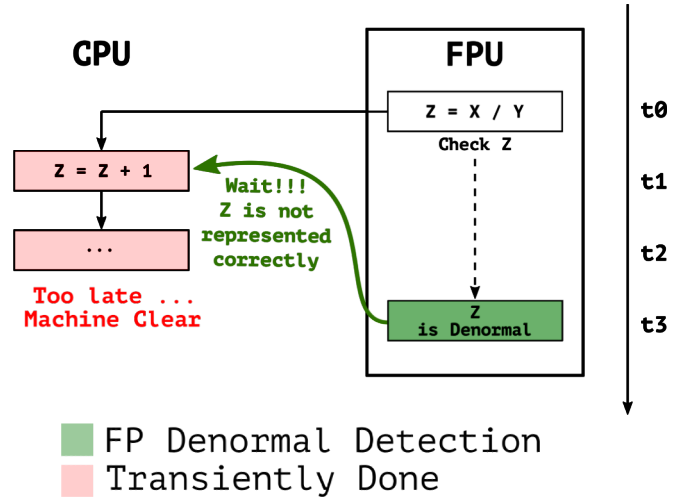
Floating-Point Value Injection (FPVI)

- Exploit leakage rate of 13 KB/s



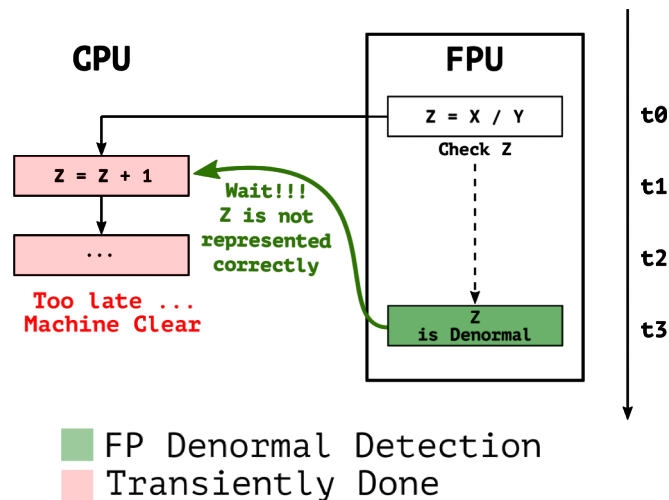
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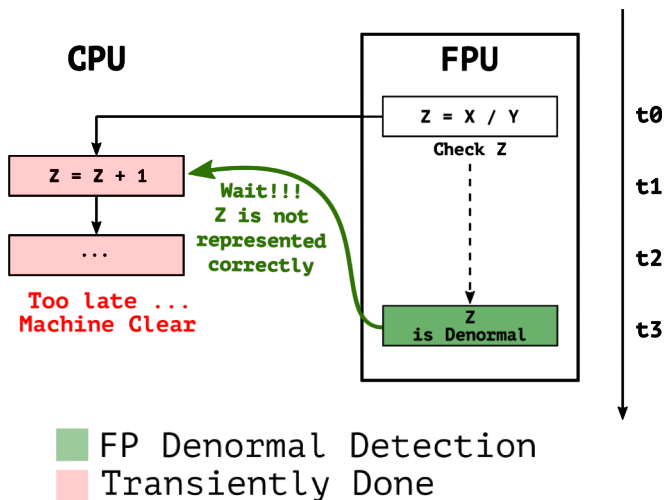
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With 53% geomean overhead for SPEC FP 2017.

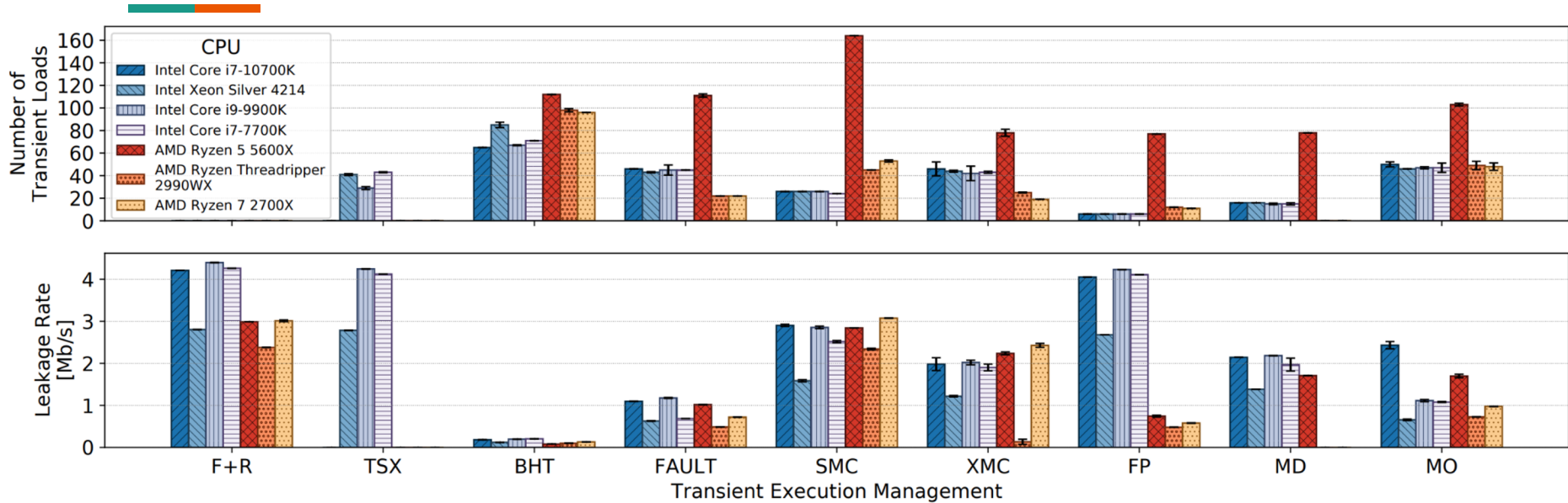


Floating-Point Value Injection (FPVI)

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 - Flush To Zero (FTZ) & Denormal Are Zero (DAZ)
 - We implemented a LLVM pass adding a serializing instruction in detected FPVI gadgets. With 53% geomean overhead for SPEC FP 2017.
 - Use site-isolation or conditionally mask FP operations in the browsers.



Transient Execution Capabilities

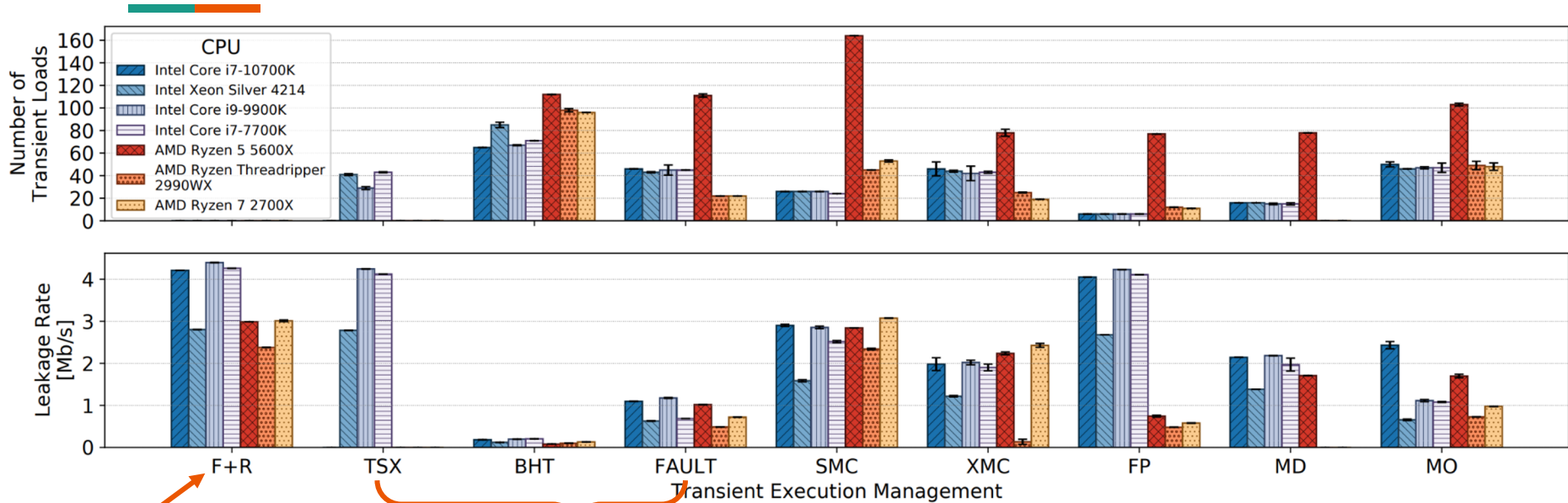


Transient Execution Capabilities



Architectural
baseline
leakage rate

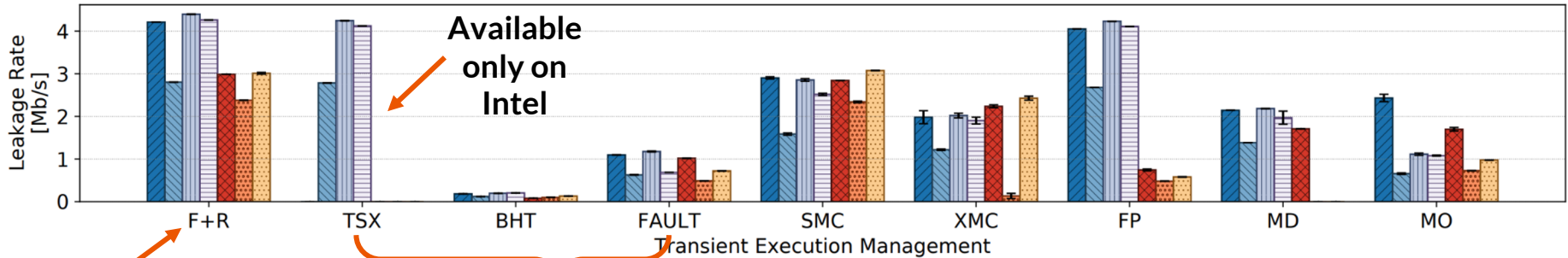
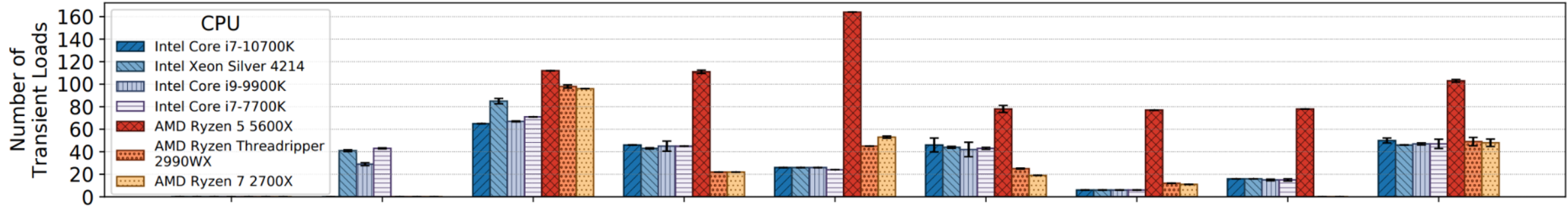
Transient Execution Capabilities



Architectural
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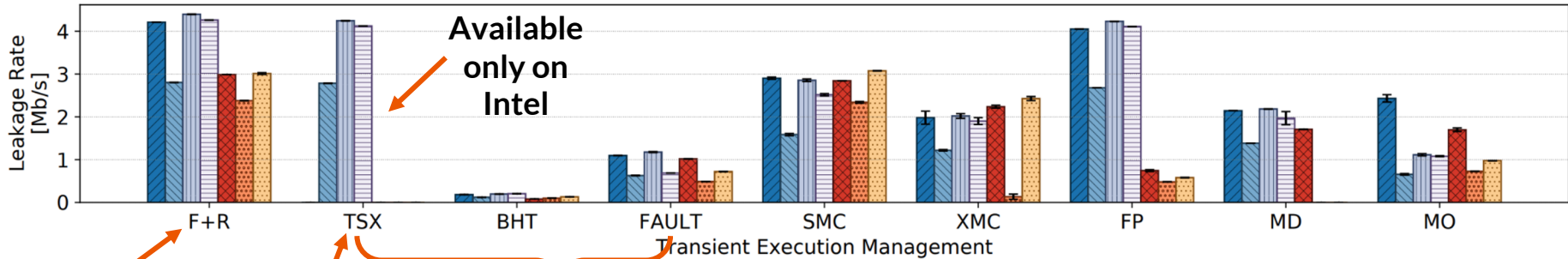
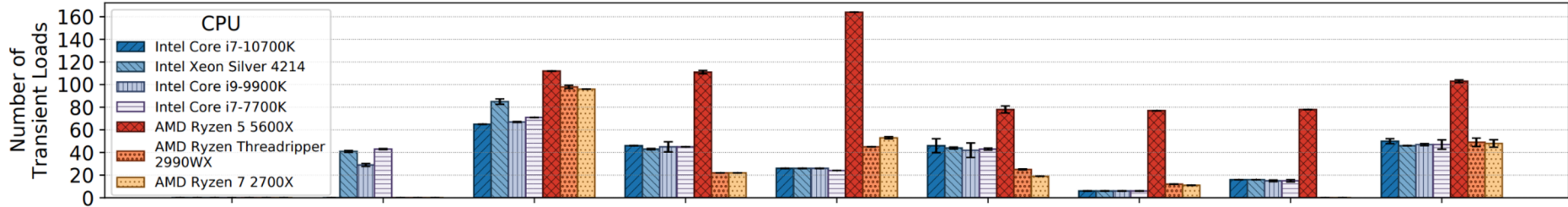
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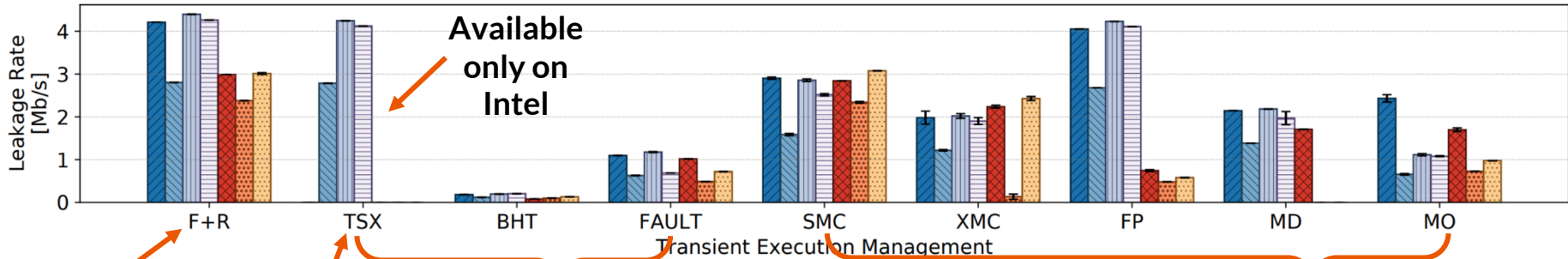
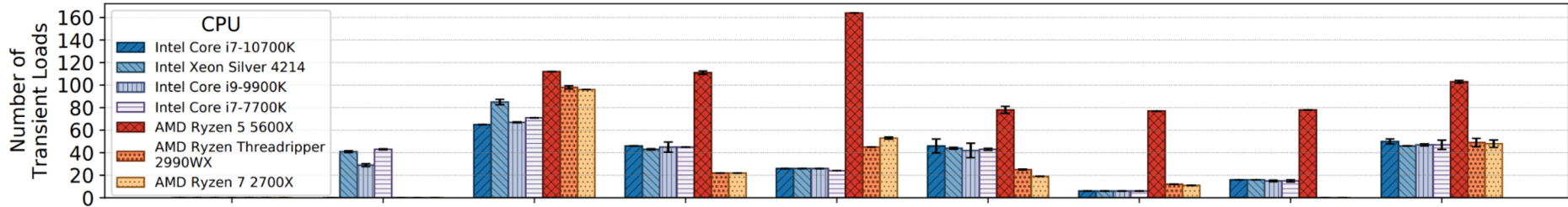


Architectural baseline leakage rate

Not supported anymore on recent CPUs



Transient Execution Capabilities



Available only on Intel

Architectural baseline leakage rate

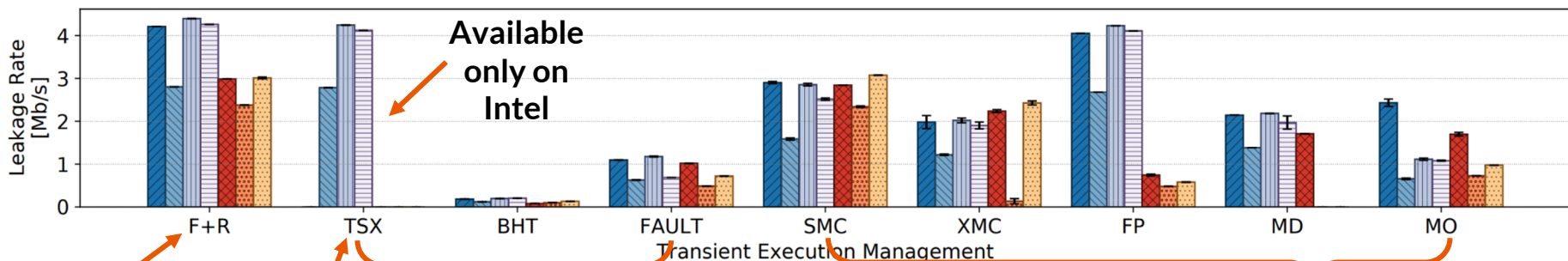
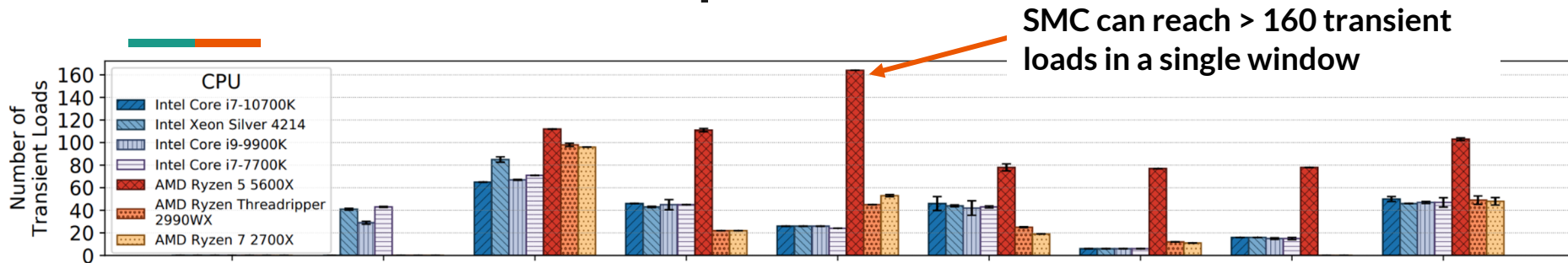
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Transient Execution Management

Available also on AMD

Transient Execution Capabilities



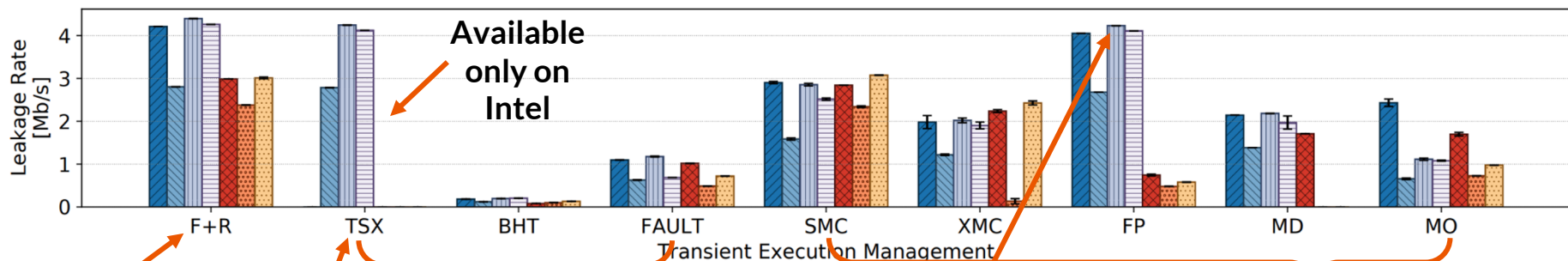
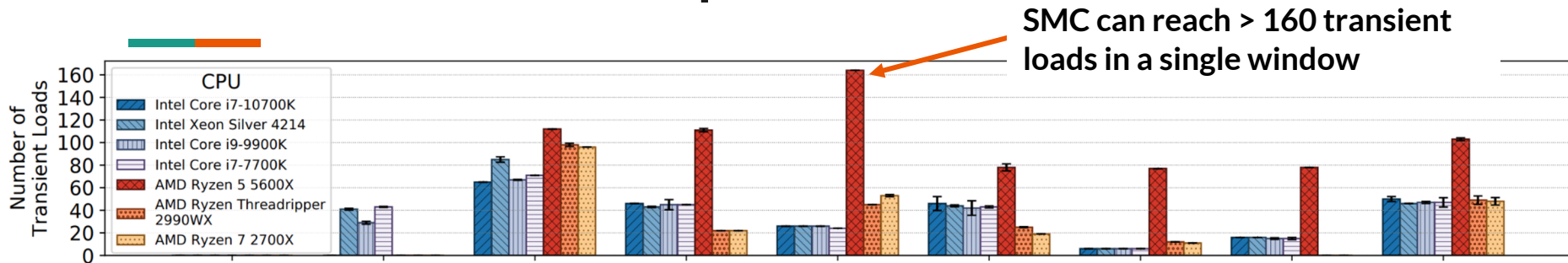
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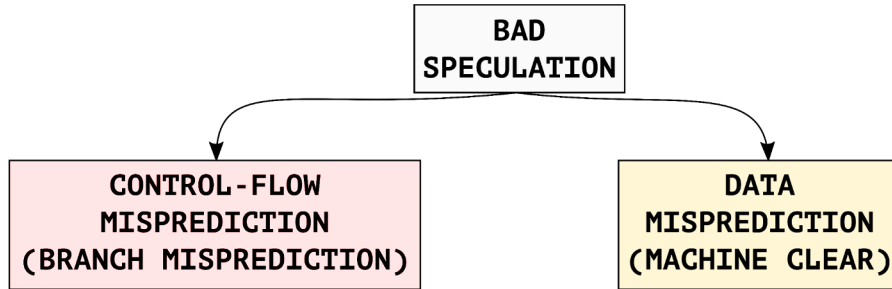
FP has the best leakage rates (>4Mb/s) thanks to its determinism (i.e. No mistraining needed)

Available also on AMD

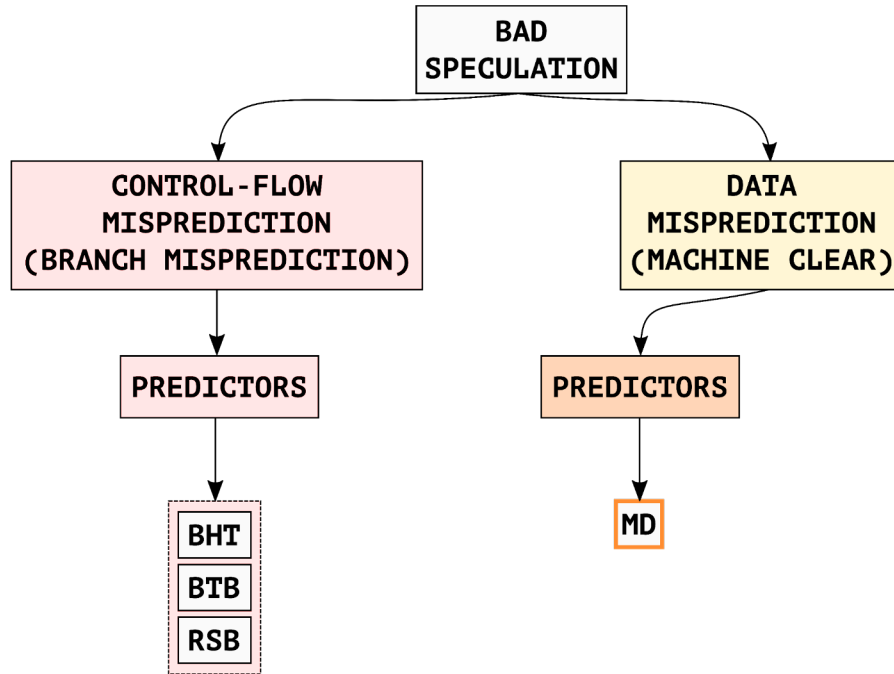
Root-Cause Classification of Transient Execution



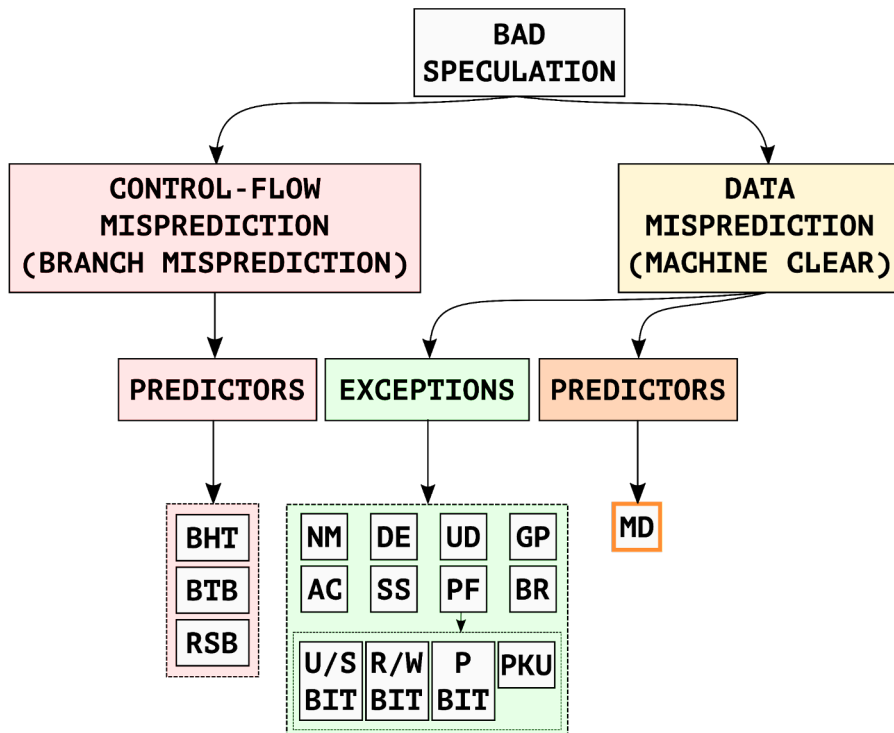
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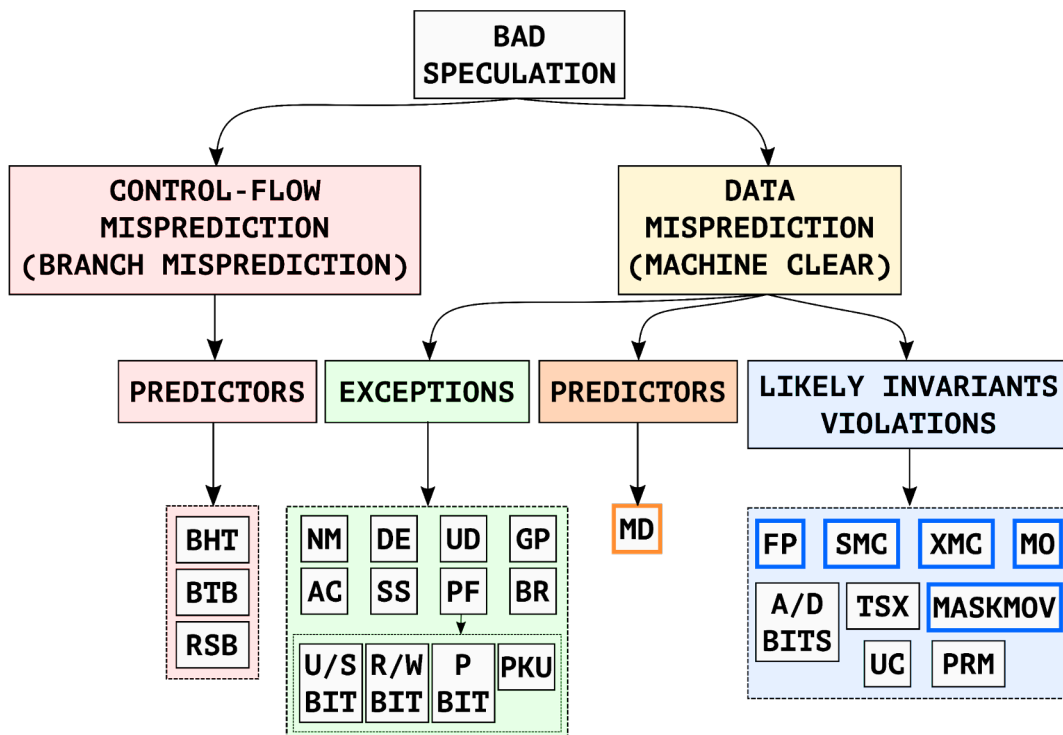
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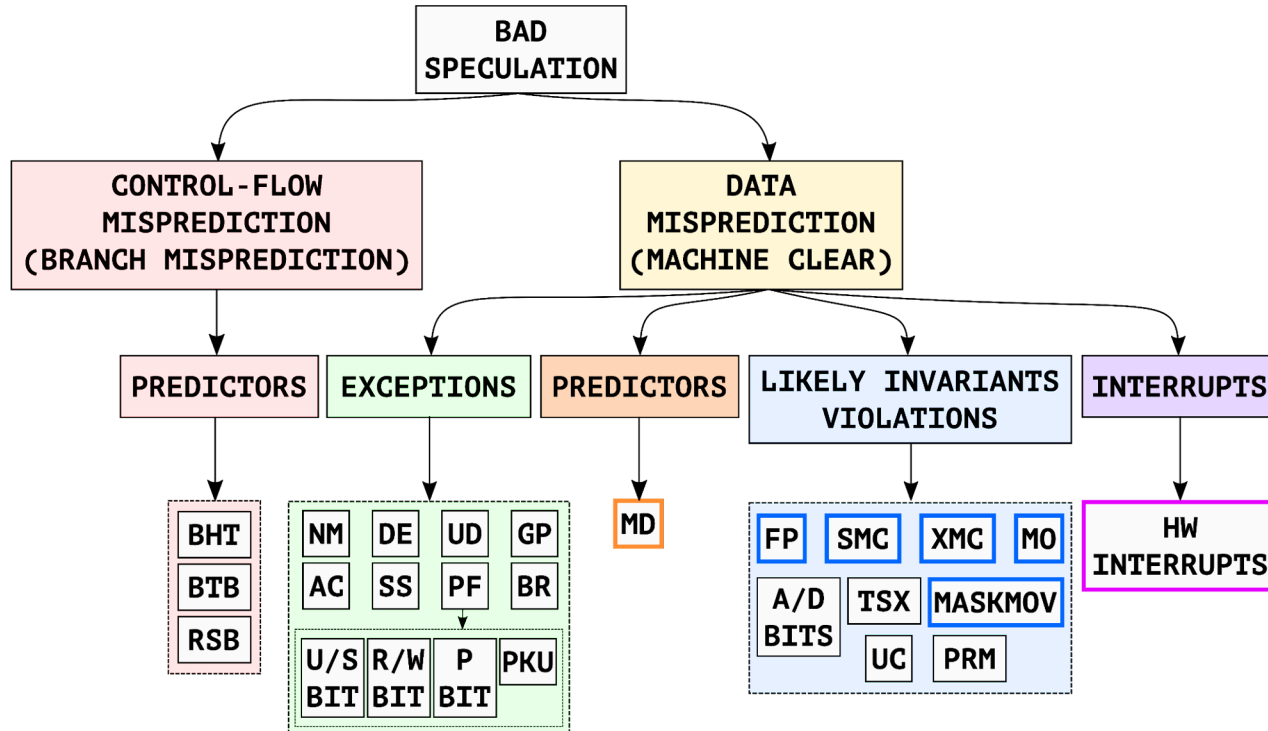
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Root-Cause Classification of Transient Execution



Disclosure & Affected CPUs



- We disclosed FPVI and SCSB to CPU, browser, OS, and hypervisor vendors in February 2021.

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CPU Vendor	Affected by SCSB (CVE-2021-0089) (CVE-2021-26313)	Affected by FPVI (CVE-2021-0086) (CVE-2021-26314)
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- Xen hypervisor mitigated SCSB and released a security advisory (XSA-375) following our proposed mitigation.

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@hanyrax

@enrico_barberis

Code, exploit demo and more can be found here:

