APEX: A Verified Architecture for Proofs of Execution on Remote Devices Under Full Software Compromise

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Safety Critical Embedded/Cyber-physical/IoT Systems

● Several interconnected devices
  ○ Control units
  ○ Sensors
  ○ Actuators
  ○ Network devices

● Examples
  ○ Industrial facilities
  ○ Home automation
  ○ Vehicles

● Heterogeneous:
  Typically more sophisticated devices controlling simple low-end embedded systems
Safety Critical Embedded/Cyber-physical/IoT Systems

- **Examples**
  - Smoke detector in a household
  - Engine’s temperature sensor in a car

Controllers rely on sensed values to make decisions (e.g., send help)
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Low-End Embedded Devices, Sensors, Actuators...
(aka amoebas of the computing world)

- Designed for: **Low-Cost, Low-Energy, Small-Size.**
- Memory: Program (-32kB) and Data (-2-16 kB)
- Single core CPU (-8-16MHz; 8- or 16-bit)
- Simple Communication (I/O) Interfaces (a few kbps)
- Examples: TI MSP-430, AVR ATmega32 (Arduino)
Problem at Hand

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○ Can we do this cost-effectively? Even if all software on a device can be modified and/or compromised at any point in time?
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Or: Can we build sensors that “cannot lie”? (Even when infected)
Background: The Software Process in a Sensor

- Software on the Microcontroller triggers Sensing Hardware through General Purpose Input-Output (GPIO), according to some communication protocol, and waits for the sensed value as a response.
**Background: The Software Process in a Sensor**

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- **Sensing Hardware:**
  - Digital or Analog circuitry
  - E.g.: Resistors with variable resistance according to temperature, pressure, light, etc.

- **GPIO:**
  - Memory addresses connected to physical ports in the Microcontroller.
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Trustworthy Sensing: Prove that a value was indeed obtained from the expected GPIO interface, via execution of the expected software.
Previous Work on Securing the Software-State of Low-End Embedded Systems

- Typically involves some form of **Remote Attestation (RA)**:
  - A general approach of detecting malware presence on invalid software state on devices
  - Two-party interaction between:
    - **Verifier**: trusted entity
      - (e.g., a higher-end controller device in a CPS)
    - **Prover**: potentially infected and untrusted remote IoT device
      - (e.g., a low-end sensor/actuator)
  - Goal: measure current internal state (the contents in memory) of **prover**
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**Examples of RA for Low-End Devices:** SMART[NDSS’12], SANCUS[SEC’12], Trustlite[EuroSys’14], Tytan[DAC’15], Hydra[WiSec’17], VRASED[Sec’19], …
Remote Attestation Interaction

Verifier

Prover

(1) Challenge

(3) Response

(2) Response = authenticated challenge-based measurement (via some cryptographic integrity-ensuring function)

Often implemented as a Message Authentication Code (MAC) over prover’s memory

(4) Verify response, decide outcome
Remote Attestation Interaction

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If secure should provide an unforgeable proof that the Prover’s memory corresponds to a given value at the time of RA computation
Natural Path: Use RA to Build Sensors that “Cannot Lie”

- However… RA by itself is not sufficient
  - Does not prove execution of attested code
  - Does not bind the outputs to the execution of the code
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For example, attempts using a regular RA architecture:
- **Attest-then-Execute:**
  - Vulnerable to: Attest $\xrightarrow{}$ Compromise $\xrightarrow{}$ Execute
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  - **Execute-then-Attest:**
    - Vulnerable to: Compromise → Execute → Heal → Attest
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- Execute-then-Attest:
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  - **Attest-then-Execute-then-Attest:**
    - Vulnerable to: Attest → Compromise → Execute → Heal → Attest

Clever Malware hides itself! Not possible to prove that the proper code executed!

**Takeaway:** Even ideal secure RA functionality, by itself, is not sufficient! We need a proof of execution of the expected code tied to any produced output.
Proofs of (Remote Software) EXecution (PoX)
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  - Executed code
  - Outputs produced by this execution
  - Temporally consistent remote attestation of the executed code and respective outputs
- Extension to the RA capability
**Proofs of (Remote Software) EXecution (PoX)**

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- Extension to the RA capability
- **Reminder!** We must be mindful of:
  - Low-cost, low-energy, small-size
  - Possibility of full software compromise
    - Implies some hardware support!
Realizing PoX with APEX

- APEX: (Formally Verified) Architecture for Proofs of Execution
Realizing PoX with APEX

- **APEX:** (Formally Verified) Architecture for Proofs of Execution
- **Idea:**
  - With cost in mind... The simplest thing we can do is to set one bit
  - This bit is referred to as “EXEC flag”
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  ○ EXEC flag is stored in a fixed physical memory address that is covered by the RA measurement.

● Assuming a secure underlying RA architecture, unforgeability guarantees that the attestation result must reflect the actual value of EXEC during the RA computation
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What does “proper execution” mean?
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What does “proper execution” mean?

- In this work:
  1 - Executable **runs atomically** (i.e., uninterrupted), **from its first instruction, until its last instruction**.
  2 - Execution happens after receiving the latest attestation challenge
     - **Timeliness. No replayed PoX!!!**
  3 - Neither the Executable, nor its Outputs (if any) are modified in between the execution and subsequent RA computation.
APEX Design
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APEGX Design

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  - Pointers to the location of the executable
    - Executable Range (ER)
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    ■ Output Range (OR)
  ○ Pointers to the location of the executable
    ■ Executable Range (ER)

APEX hardware module controls EXEC value based on the parameters in METADATA and several CPU signals.


APEX Design

- **Before execution:**
  - Execution configuration must be written to METADATA before execution
    - Including the challenge!
AEPX Design

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  - METADATA **cannot be changed** once execution starts!
    - Any change to METADATA at any point causes EXEC=0
    - Necessary for PoX security
    - More on this later...
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  ○ METADATA cannot be changed once execution starts!
    ■ Any change to METADATA at any point causes EXEC=0
    ■ Necessary for PoX security
    ■ More on this later...
  ○ Configuration parameters can be written by untrusted software running on the Prover (i.e., the low end device), however:
    ■ Must specify ER to be the region actually containing the proper executable
    ■ Must specify OR sufficiently large to fit the expected output
    ■ Otherwise PoX will fail
      ● More on this later...
APEX Design

- During execution:
  - Initially $\text{EXEC}=0$ (default value, e.g., after boot or a reset)
Attested Memory

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    - Program counter (PC) must point to the first instruction of ER (as determined in METADATA)
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    - Program counter (PC) must point to the first instruction of ER (as determined in METADATA)
  - If any of the following happens **before PC reaches the last instruction of ER**, APEX sets **EXEC=0**:
    - **Interruption**: irq, reset, PC $\notin$ ER, etc...
      - Gives Malware opportunity to skip instructions, change intermediate execution data, outputs etc.
    - **DMA activity**: Could tamper with intermediate execution results in data memory and OR, or change instructions in ER.
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Key Observations:
1- The only way to leave ER’s execution with EXEC=1 is by running ER in its entirety (until its last instruction)!
2- In order to bind the execution to the produced output, ER must write outputs to OR (as configured in METADATA)!
APEX Design

- After execution:
  - Honest Prover: Calls attestation. Memory is set to produce a valid PoX for execution of ER with output OR
  - Recall: RA covers METADATA, ER and OR.
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    ■ Modify ER:
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  - Modify OR:
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      - Use this execution proof with future challenges (execution replay attack!)
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    - Modify METADATA to change ER/OR addresses:
      - Make it look like a valid proof of execution of some other ER, somewhere else in memory.
      - Make it look like this execution produced some other result, stored somewhere else in memory.
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APEX hardware module monitors for such actions setting EXEC=0 if any of them happen!
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3. Install the received code in the defined location
4. Setup configuration registers (e.g., “where to store the output” among others)
5. Execute the installed code
6. Call VRASED attestation functionality (locations to be attested defined according to step 4 above).
Meanwhile APEX verified hardware monitors steps 3 to 6:
- Controls the value of a 1-bit flag "EXEC".
  - IMPORTANT: EXEC is read-only to all software.
  - EXEC=1 if and only if steps 3 to 6 happen securely:
    - If untrusted software misbehaves in 3 to 6; EXEC=0.
    - Several important details to the meaning of "securely" omitted in this presentation.
- EXEC value and the execution output are also covered by VRASED's attestation (in addition to the executed code).
**APEX Interaction Summary**

**Verifier**
1. Define execution METADATA
2. Send METADATA
3. Verify O and H

**Prover**
1. Send METADATA
2. Install received code to proper location
3. Set up configuration registers (located in protected memory) according to the other parameters in METADATA
4. Execute received software, producing output O
5. Output H

**APEX HW**
Monitor steps: 3, 4, 5, 6

**VRASED’s Attestation**
6. Invoke
7. Compute H

**VRASED’s Attestation produces result H:**
- Attestation result H is sent back to the Verifier along with output O.
- Both “EXEC” flag and are O are covered by VRASED’s attestation.
- **Verifier will only accept H reflecting EXEC=1.**
- Therefore, Prover can not produce pair (H, O) that will be accepted by the verifier unless:
  - O was indeed produced by the execution expected software (as defined in METADATA).
  - Cryptographic challenge ensure freshness of the execution (i.e., no replay of previous executions/results).
APEX Verification
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- Formal Verification: Why bother?
  - Formal specification:
    - Provides unambiguous logical expressions to state APEX sub-properties avoiding misinterpretation of requirements.
  - Did we get it right?
    - Once properties are formally specified, the hardware design can be proved to adhere to such properties (computer aided verification via model checking)
  - Are these properties enough?
    - Many properties... we could be missing something!
    - Can use theorem proving to show that the conjunction of all properties, when applied to the low-end device machine model implies an end-to-end notion of secure PoX.
**APEX Sub-Properties Formally**

**Definition 7. Necessary Sub-Properties for Secure Proofs of Execution in LTL.**

**Ephemerality Immutability:**

\[ G : \{ [W_{en} \land (D_{addr} \in ER)] \lor [DMA_{en} \land (DMA_{addr} \in ER)] \to \neg EXEC \} \]  

(3)

**Ephemerality Atomicity:**

\[ G : \{ (PC \in ER) \land \neg (X(PC) \in ER) \to PC = ER_{max} \lor \neg X(EXEC) \} \]  

(4)

\[ G : \{ \neg (PC \in ER) \land (X(PC) \in ER) \to X(PC) = ER_{min} \lor \neg X(EXEC) \} \]  

(5)

\[ G : \{ (PC \in ER) \land \text{irq} \to \neg EXEC \} \]  

(6)

**Output Protection:**

\[ G : \{ \neg (PC \in ER) \land (W_{en} \land D_{addr} \in OR)) \lor (DMA_{en} \land DMA_{addr} \in OR) \lor (PC \in ER \land DMA_{en}) \to \neg EXEC \} \]  

(7)

**Executable/Output (ER/OR) Boundaries & Challenge Temporal Consistency:**

\[ G : \{ ER_{min} > ER_{max} \lor OR_{min} > OR_{max} \to \neg EXEC \} \]  

(8)

\[ G : \{ ER_{min} \leq CR_{max} \lor ER_{max} > CR_{max} \to \neg EXEC \} \]  

(9)

\[ G : \{ ([W_{en} \land (D_{addr} \in METADATA)] \lor [DMA_{en} \land (DMA_{addr} \in METADATA)] \to \neg EXEC \} \]  

(10)

**Remark:** Note that Chal_{mem} \in METADATA.

**Response Protection:**

\[ G : \{ \neg EXEC \land X(EXEC) \to X(PC = ER_{min}) \} \]  

(11)

\[ G : \{ \text{reset} \to \neg EXEC \} \]  

(12)

---

Formalized using Linear Temporal Logic (LTL)

Hardware compliance verified using NuSMV

Check APEX paper for details
The conjunction of APEX properties are shown to imply the following LTL Statement:

Definition 5. Formal specification of APEX’s correctness.

\[
\begin{align*}
\{ & PC = ER_{min} \land [(PC \in ER \land \neg Interrupt \land \neg reset \land \neg DMA_{en}) \land \mathcal{U} PC = ER_{max}] \\
& [(\neg Modify\_Mem(ER) \land \neg Modify\_Mem(METADATA) \land (PC \in ER \lor \neg Modify\_Mem(OR))) \land \mathcal{U} PC = CR_{min}] \\
& \} \quad B \quad \{EXEC \land PC \in CR\}
\end{align*}
\]

- The notion of Secure PoX is formalized as a Security Game
- APEX is hardware is composed into VRASED formally verified RA architecture [Sec’19]
- The composition is shown to imply Secure PoX, as long as
  1- VRASED is a secure RA Architecture (RA Security Game), and
  2- The above LTL statement holds.

See APEX paper for formal definitions and proof details.
Implementation and Evaluation
● APEX was instantiated along with VRASED on OpenMSP430 Verilog Design
● Synthesized on Basys3 FPGA
● Used to implement a fire sensor that “cannot lie”.

Publicly Available at:
https://github.com/sprout-uci/APEX
Implementation and Evaluation

- On top of VRASED:
  - 12% more Look-Up Tables
  - 2% additional registers

- Relatively inexpensive in comparison with related security services for run-time attestation, such as Control Flow Attestation (CFA).
Thank you for listening.
Questions?