APEX: A Verified Architecture for Proofs of Execution on Remote Devices Under Full Software Compromise

Ivan De Oliveira Nunes, Karim Eldefrawy, Norrathep Rattanavipanon, Gene Tsudik

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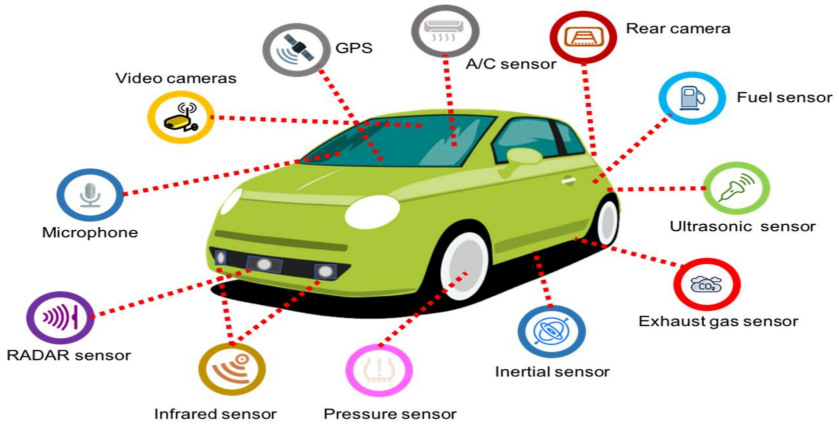
Safety Critical Embedded/Cyber-physical/IoT Systems

- Several interconnected devices
  - Control units
  - Sensors
  - Actuators
  - Network devices
- Examples
  - Industrial facilities
  - Home automation
  - Vehicles
- Heterogeneous:
  Typically more sophisticated devices controlling simple low-end embedded systems



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- Examples
  - Smoke detector in a household
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Controller
(Higher-end device)

Sensor
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<u>Controllers rely on sensed values to make decisions (e.g., send help)</u>

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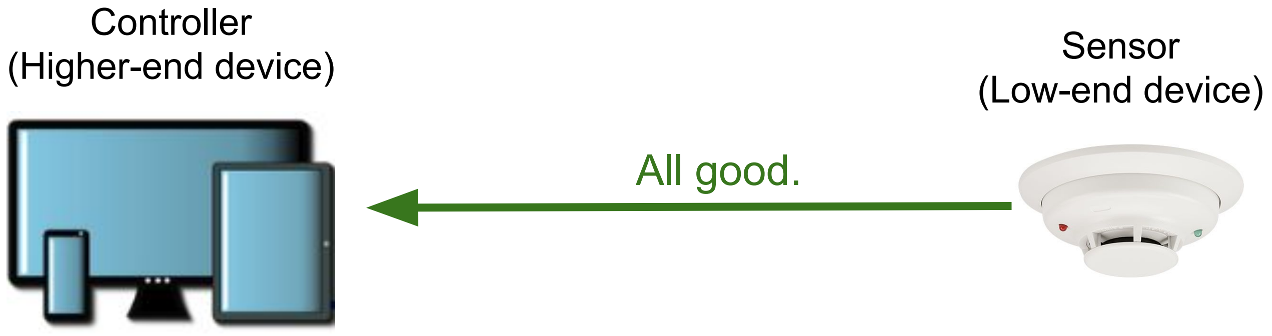

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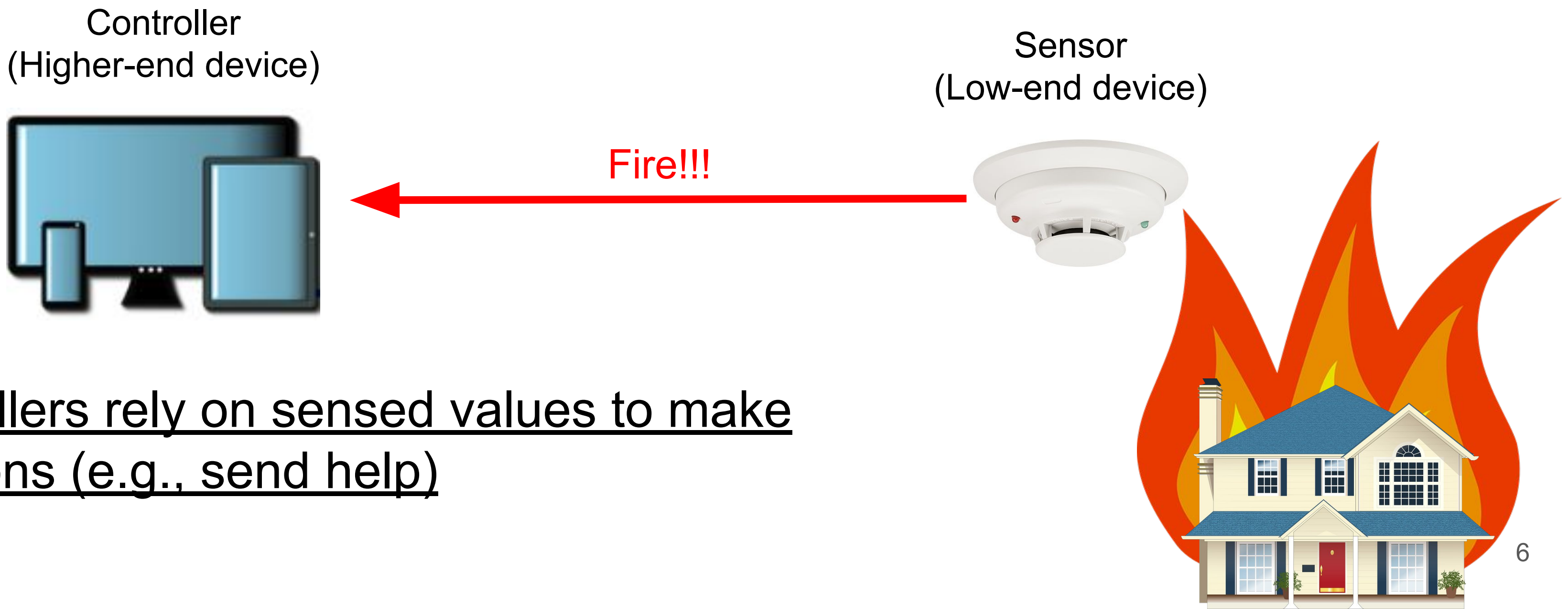

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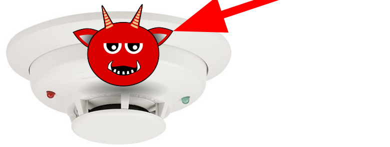

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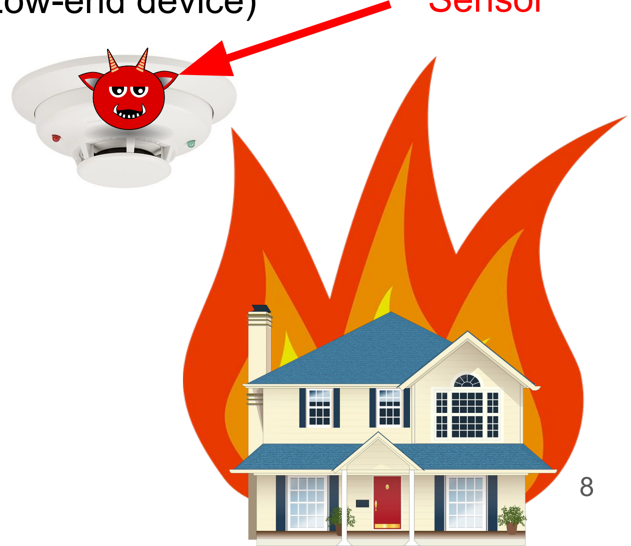
Infected
Sensor



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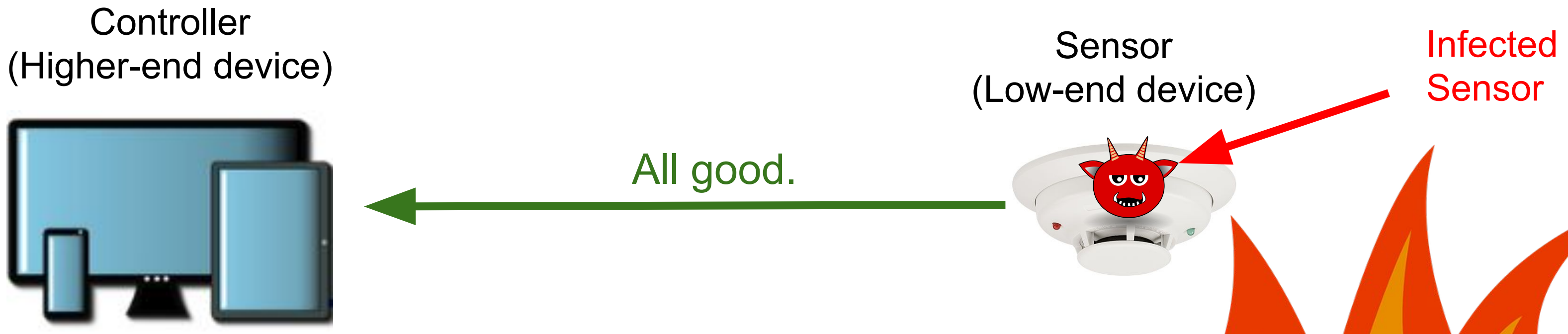

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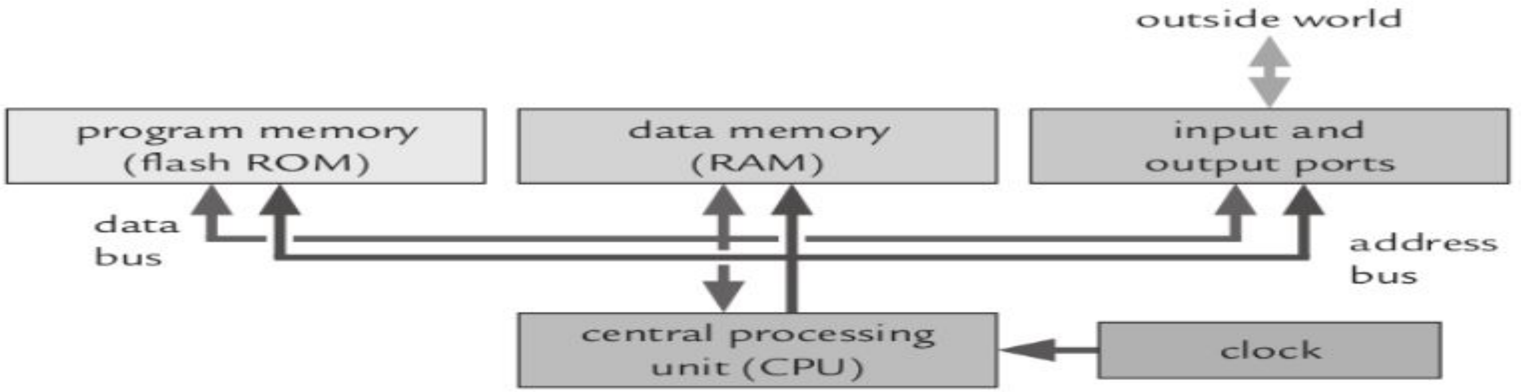
Low-End Embedded Devices, Sensors, Actuators...
(aka amoebas of the computing world)

- Designed for: **Low-Cost**, **Low-Energy**, **Small-Size.**
- Memory: Program (~32kB) and Data (~2-16 kB)
- Single core CPU (~8-16MHz; 8- or 16-bit)
- Simple Communication (I/O) Interfaces (a few kbps)
- Examples: TI MSP-430, AVR ATMega32 (Arduino)



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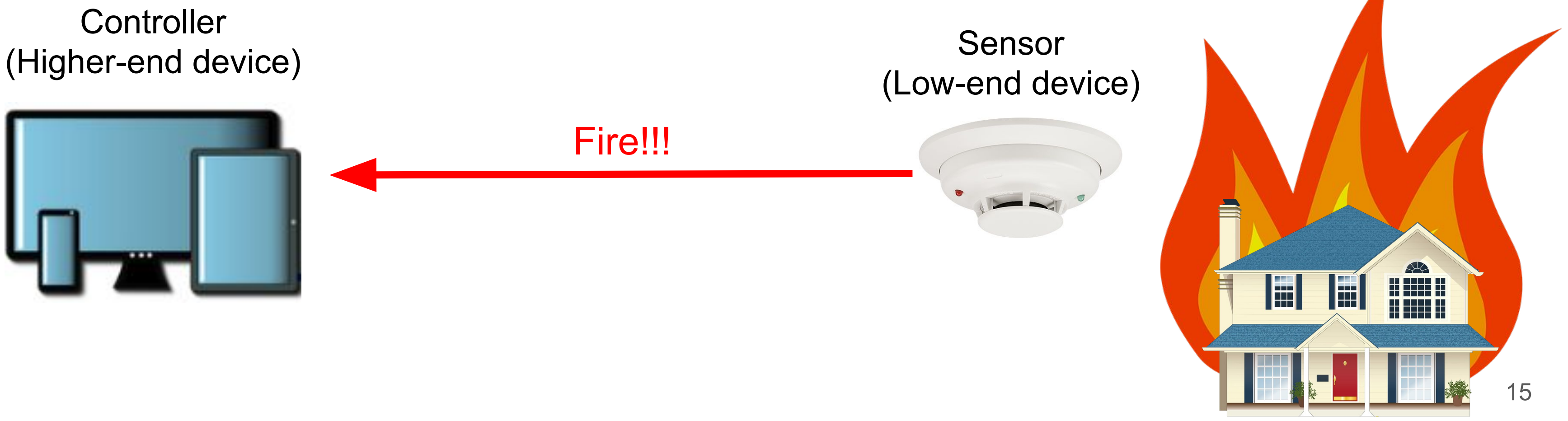

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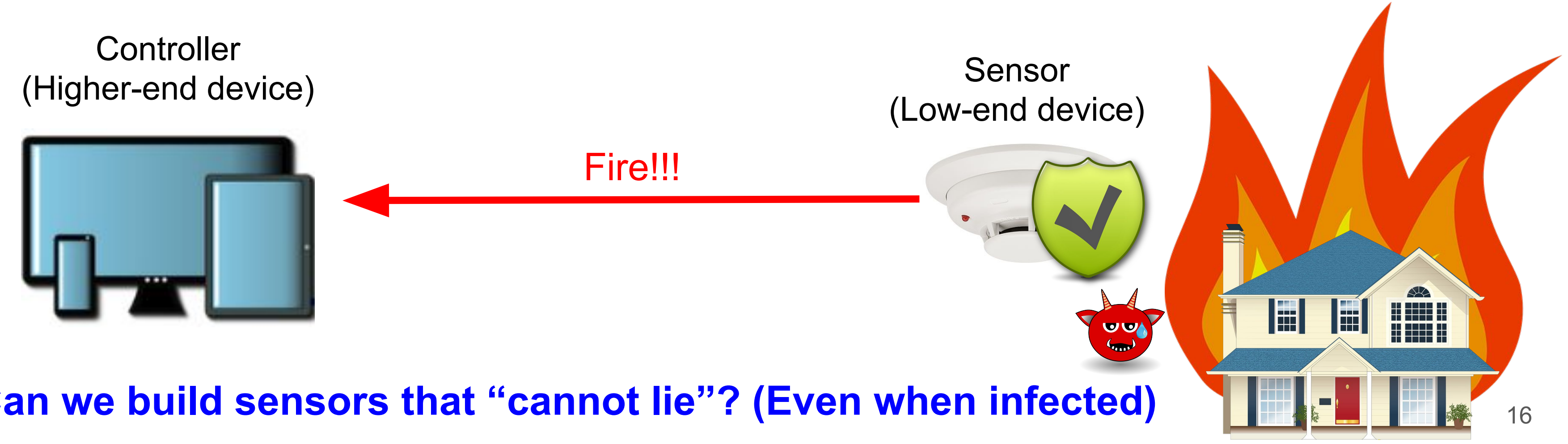

Or: Can we build sensors that "cannot lie"? (Even when infected)

Background: The Software Process in a Sensor

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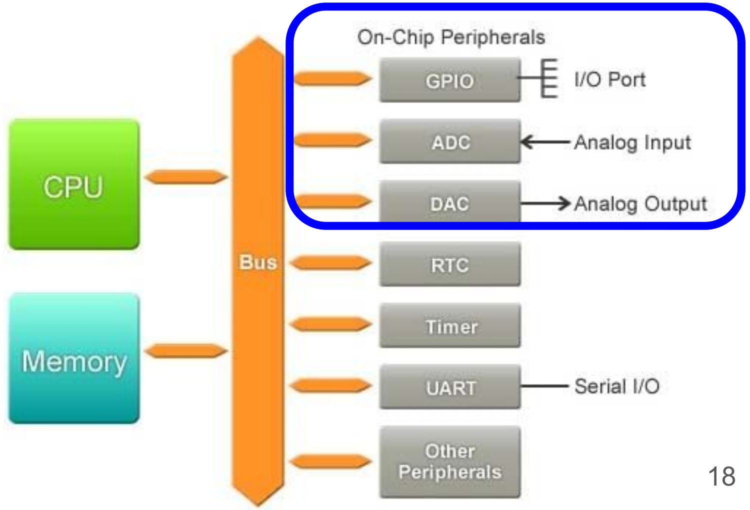
  - E.g.: Resistors with variable resistance according to temperature, pressure, light, etc.
- GPIO:
  - Memory addresses connected to physical ports in the Microcontroller.



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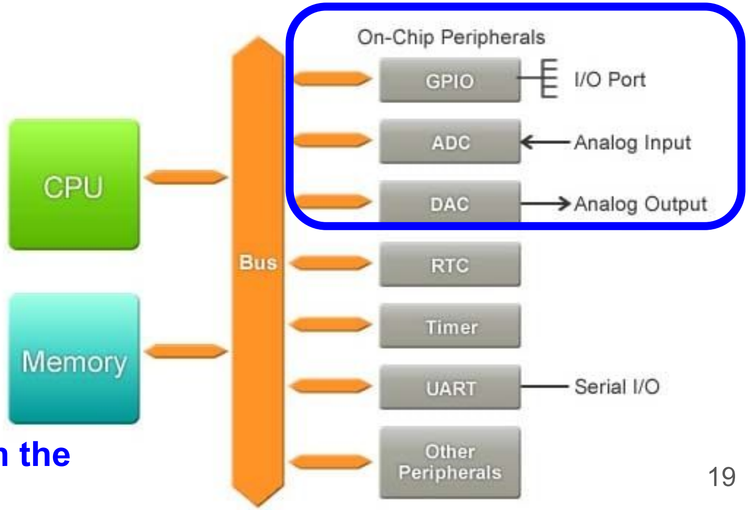

Trustworthy Sensing: Prove that a value was indeed obtained from the expected GPIO interface, via execution of the expected software

Previous Work on Securing the Software-State of Low-End Embedded Systems

- Typically involves some form of **<u>Remote Attestation (RA)</u>**:
  - A general approach of detecting malware presence on invalid software state on devices

  - Two-party interaction between:
    - **Verifier**: trusted entity
      - (e.g., a higher-end controller device in a CPS)
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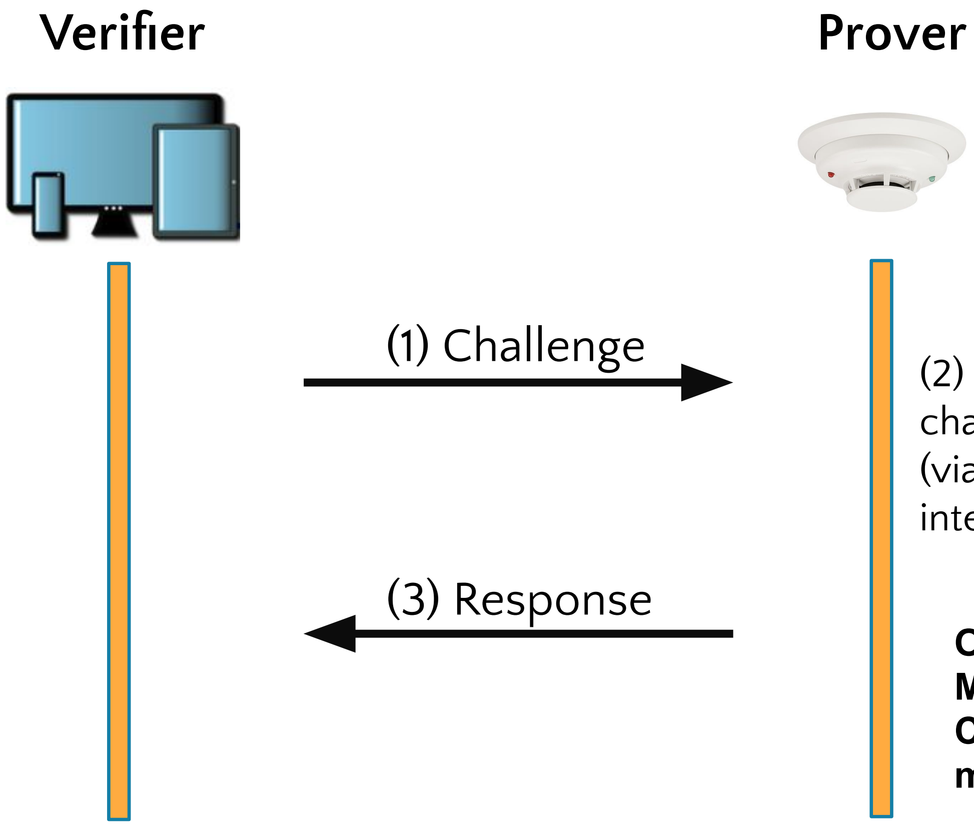
Examples of RA for Low-End Devices: SMART[NDSS'12], SANCUS[SEC'12], Trustlite[EuroSys'14], Tytan[DAC'15], Hydra[WiSec'17], VRASED[Sec'19], ...

Remote Attestation Interaction



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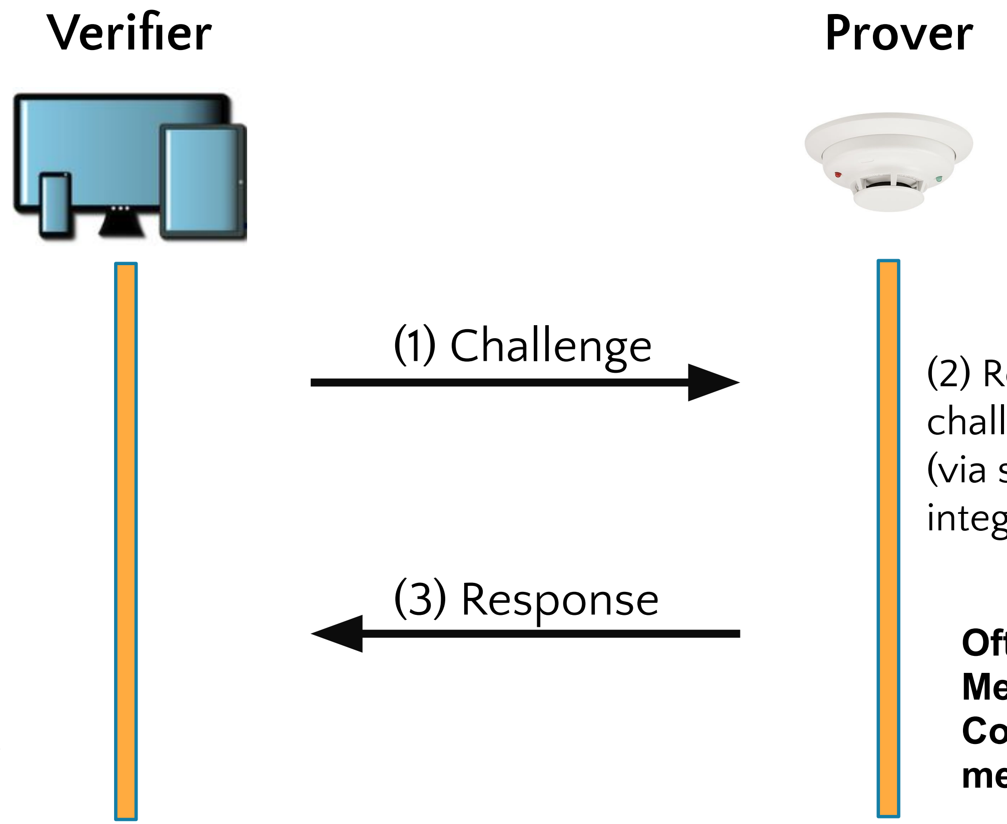

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<u>If secure</u> should provide an <u>unforgeable proof</u> that the <u>Prover's memory corresponds to a given value at the time of RA computation</u>

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Clever Malware hides itself! Not possible to prove that the proper code executed!

Takeaway: Even ideal secure RA functionality, by itself, is not sufficient! We need a proof of execution of the expected code tied to any produced output.

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- **Reminder!** We must be mindful of:
  - Low-cost, low-energy, small-size
  - Possibility of full software compromise
    - Implies some hardware support!

Sensor
(Low-end device)

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  - **`EXEC`** flag is stored in a fixed physical memory address that is covered by the RA measurement.
- Assuming a secure underlying RA architecture, unforgeability guarantees that the attestation result must reflect the actual value of **`EXEC`** during the RA computation

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  - In this work:

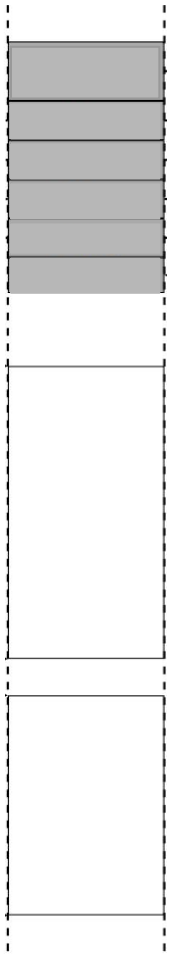
    1 – Executable **runs atomically** (i.e., uninterrupted), **from its first instruction, until its last instruction**.

    2 – Execution happens after receiving the latest attestation challenge
      - **Timeliness. No replayed PoX!!!**

    3 – Neither the Executable, nor its Outputs (if any) are modified in between the execution and subsequent RA computation.

APEX Design

Attested Memory



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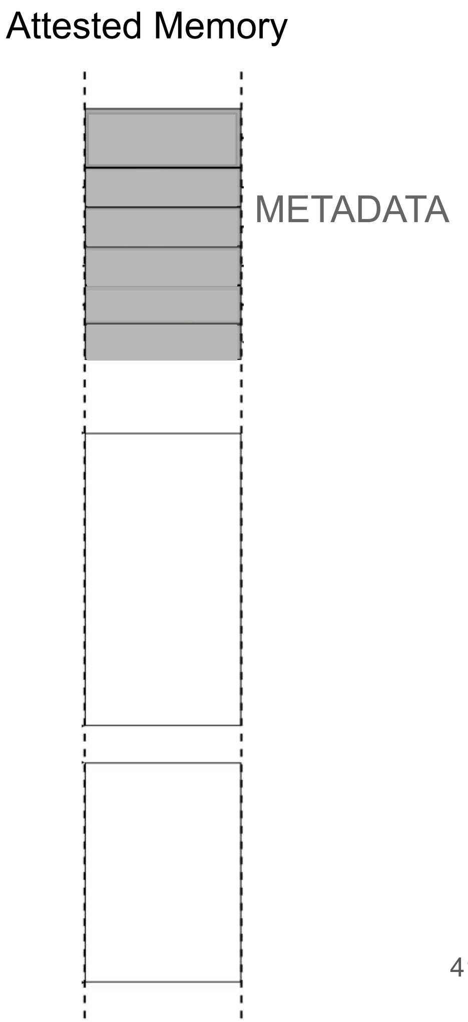

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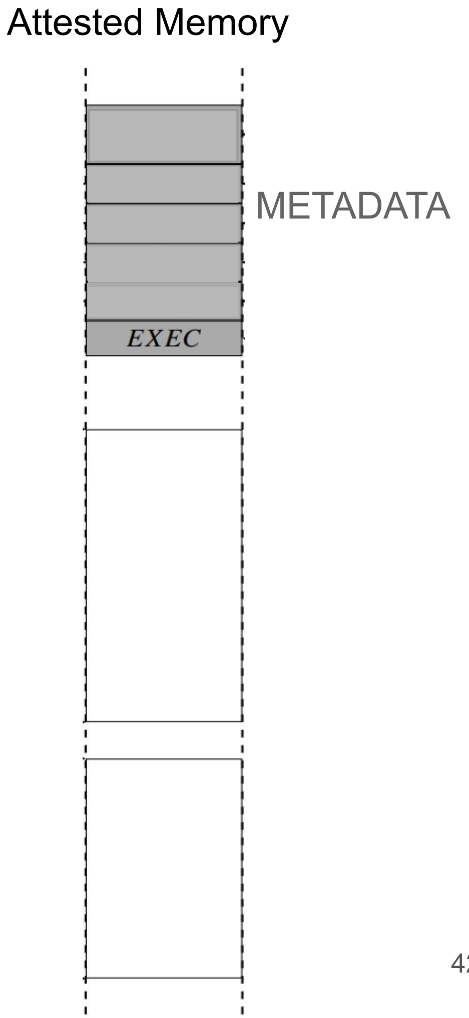

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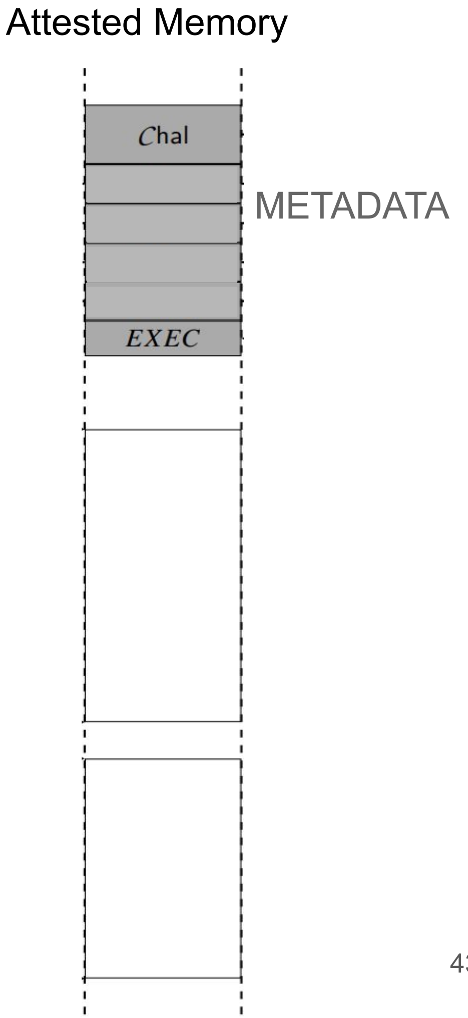

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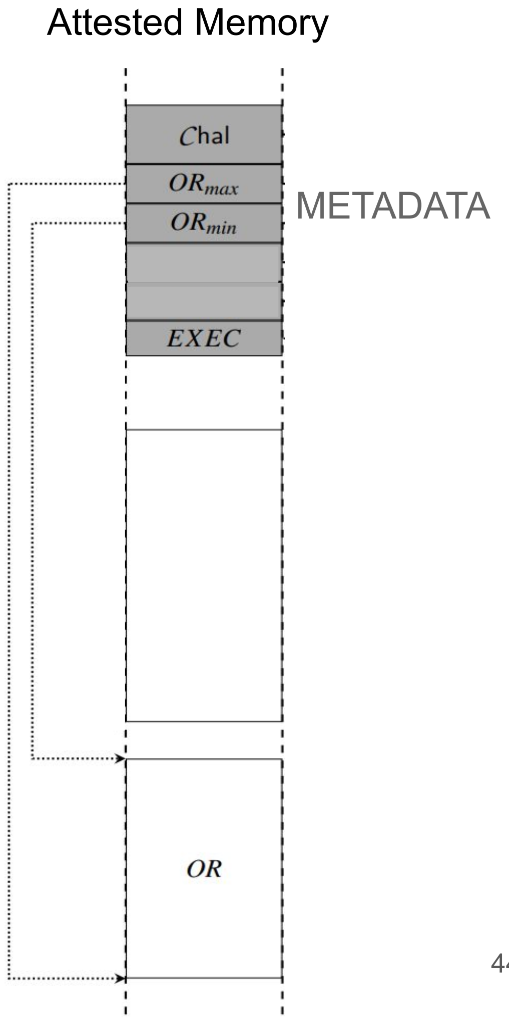

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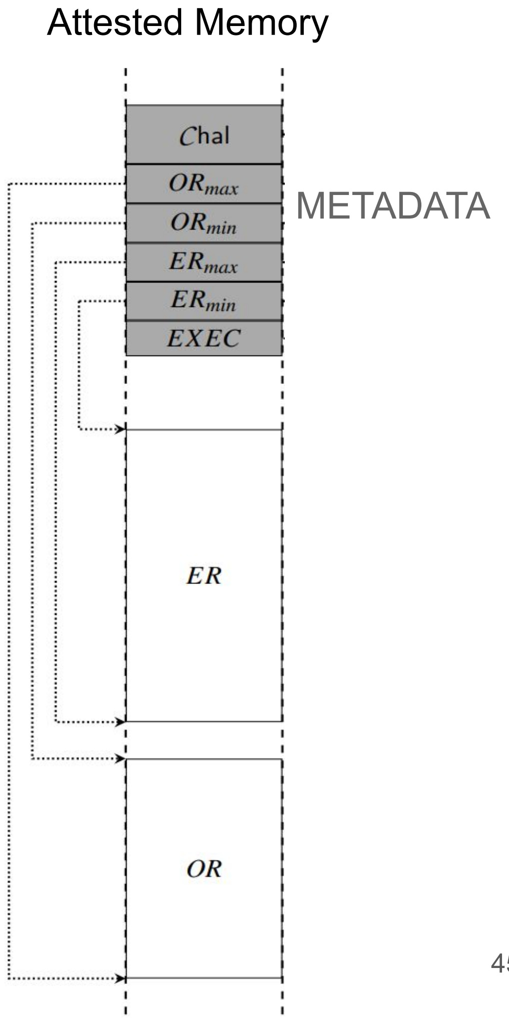

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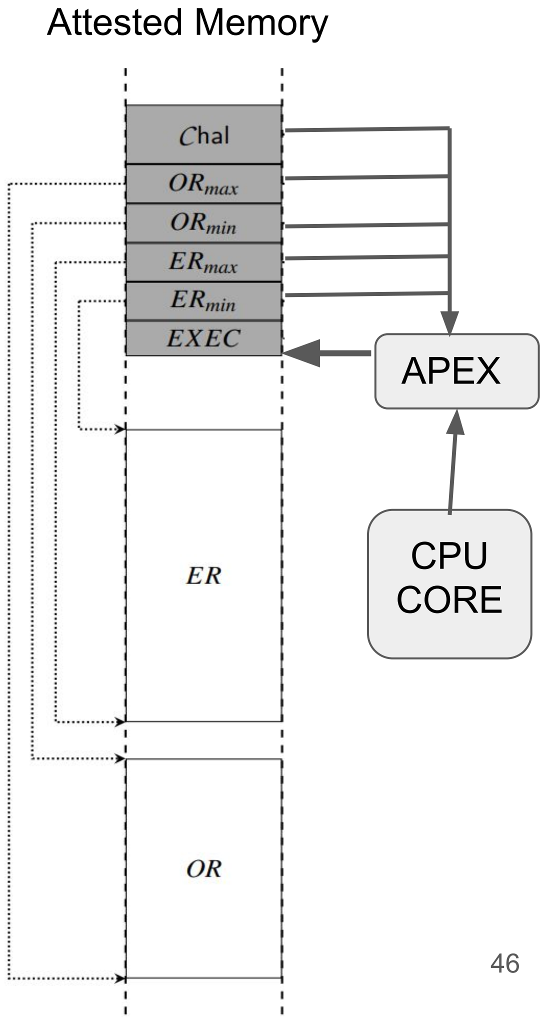
APEX hardware module controls `EXEC` value based on the parameters in METADATA and several CPU signals.



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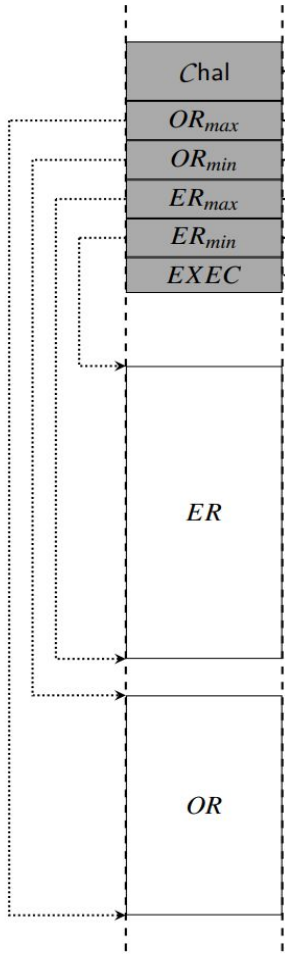

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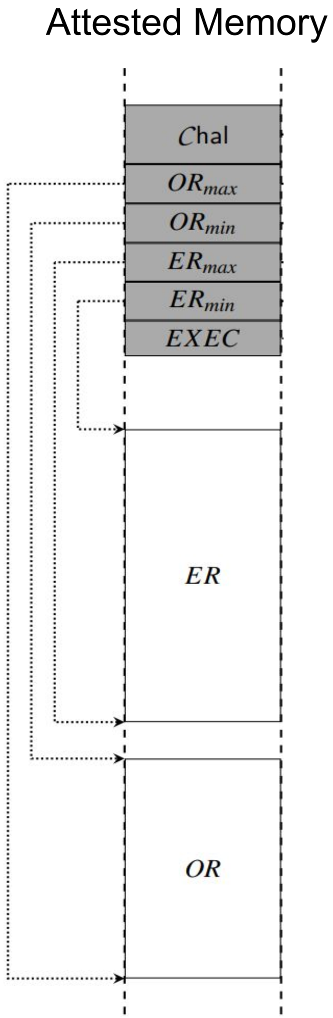

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  - Configuration parameters can be written by untrusted software running on the Prover (i.e., the low end device), however:
    - Must specify ER to be the region actually containing the proper executable
    - Must specify OR sufficiently large to fit the expected output
    - <u>Otherwise PoX will fail</u>
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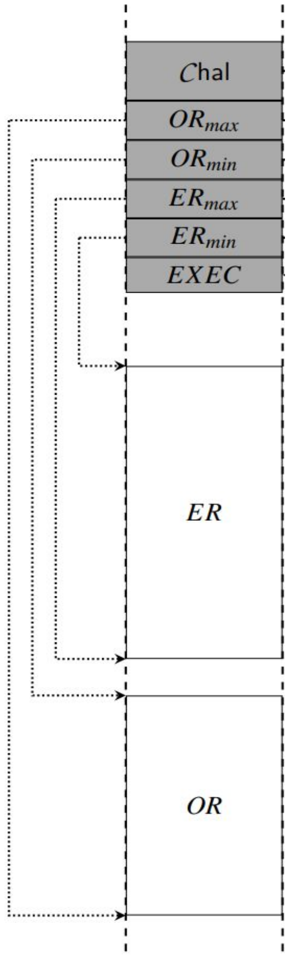

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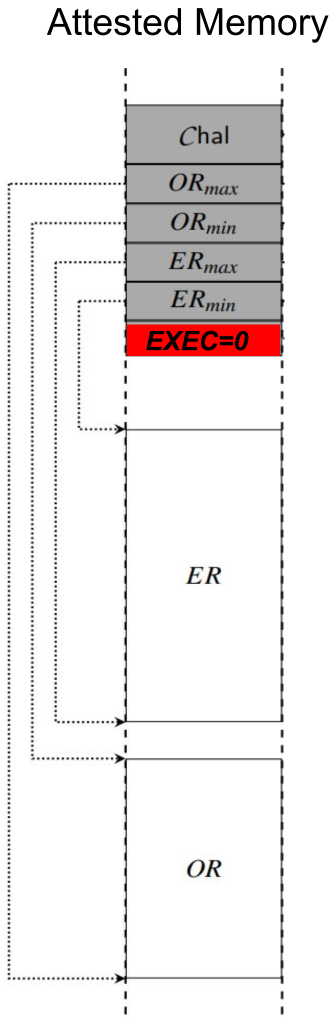

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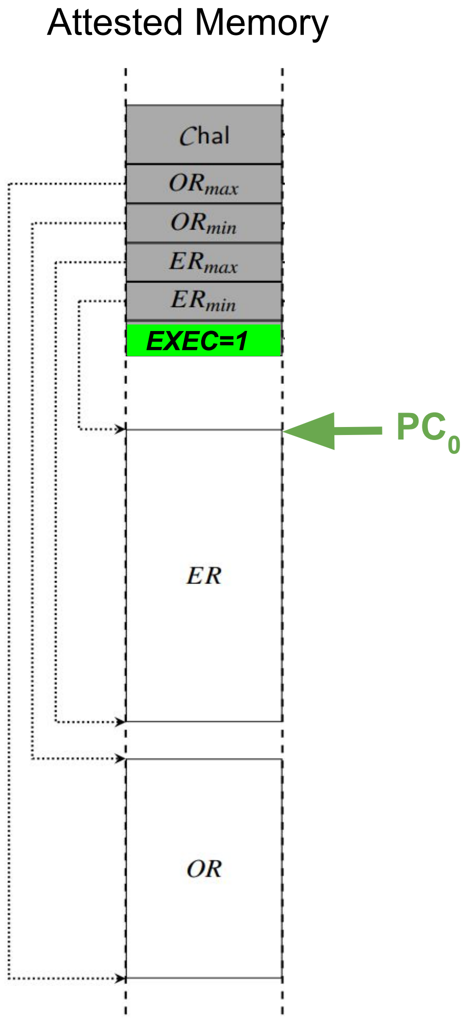

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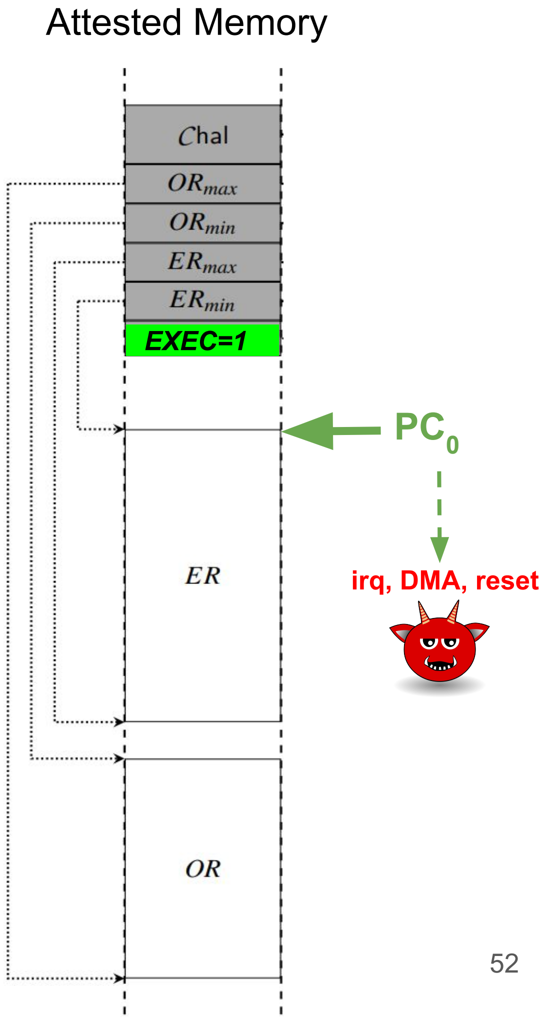

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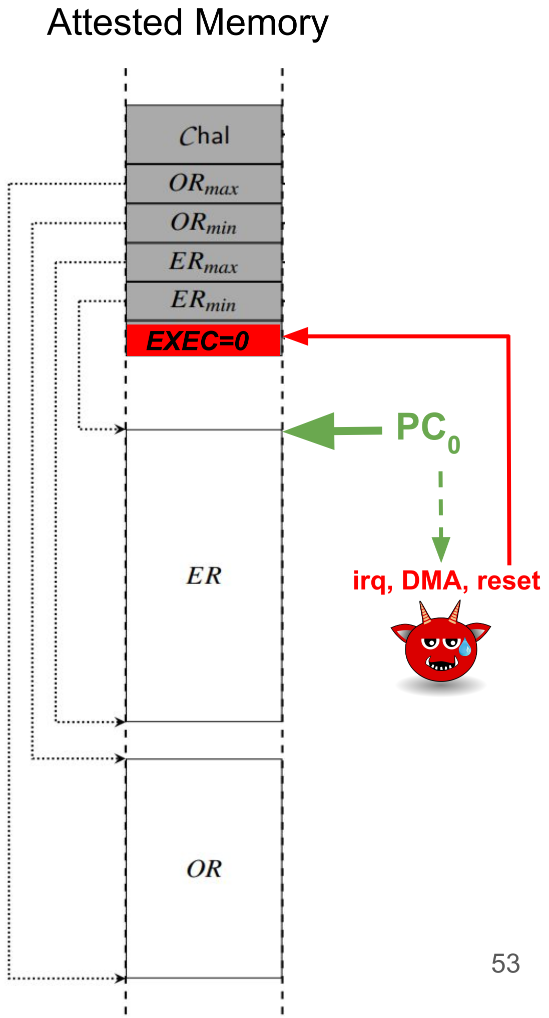

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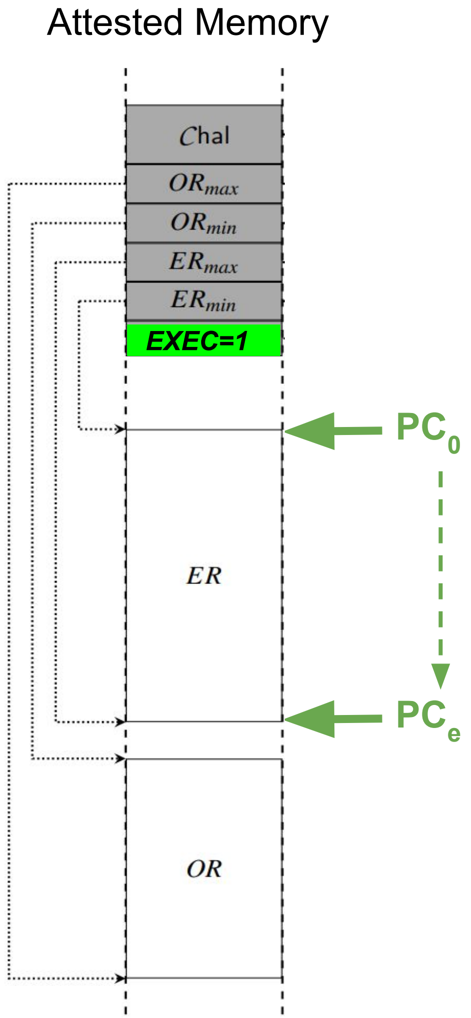


<u>**Key Observations:**</u>

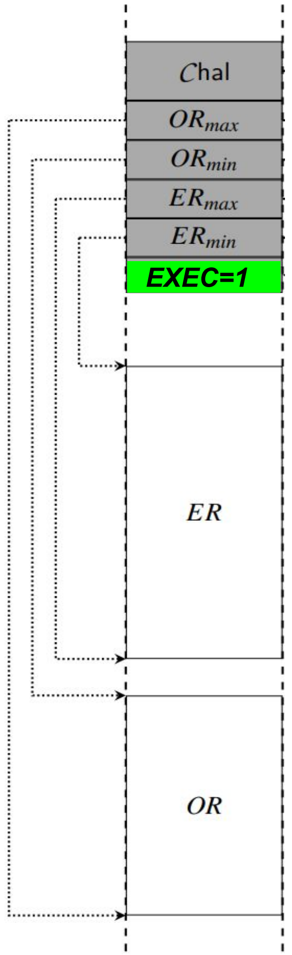
1- The only way to leave ER's execution with EXEC=1 is by running ER in its entirety (until its last instruction)!

2- In order to bind the execution to the produced output, ER must write outputs to OR (as configured in METADATA)!

APEX Design

- **After execution:**
  - **Honest Prover:** Calls attestation. Memory is set to produce a valid **PoX** for execution of <u>ER</u> with output <u>OR</u>
    - <u>**Recall:**</u> RA covers METADATA, ER and OR.

Attested Memory



APEX Design

- **After execution:**
  - **Honest Prover:** Calls attestation. Memory is set to produce a valid **PoX** for execution of ER with output OR
    - **Recall:** RA covers METADATA, ER and OR.
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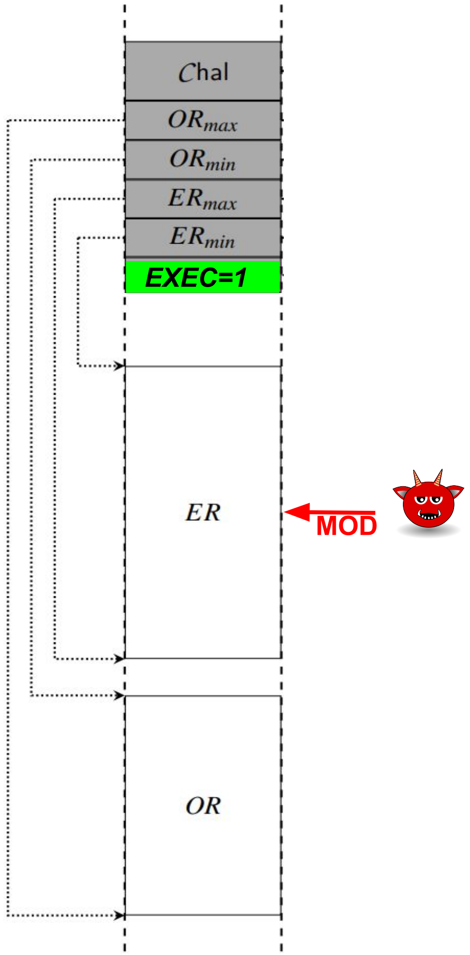
        - Maybe the execution was done with some other invalid/malicious code to begin with!

Attested Memory



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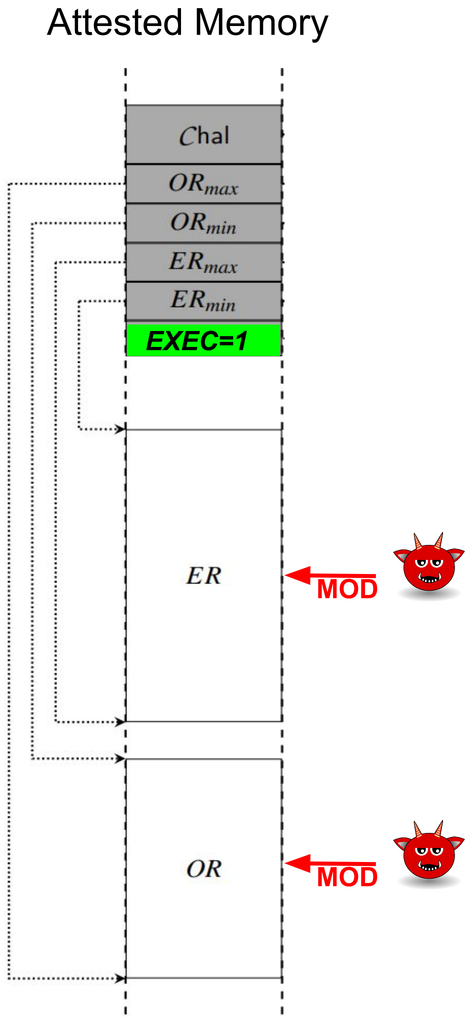
    - Modify OR:
      - Spoof the execution result



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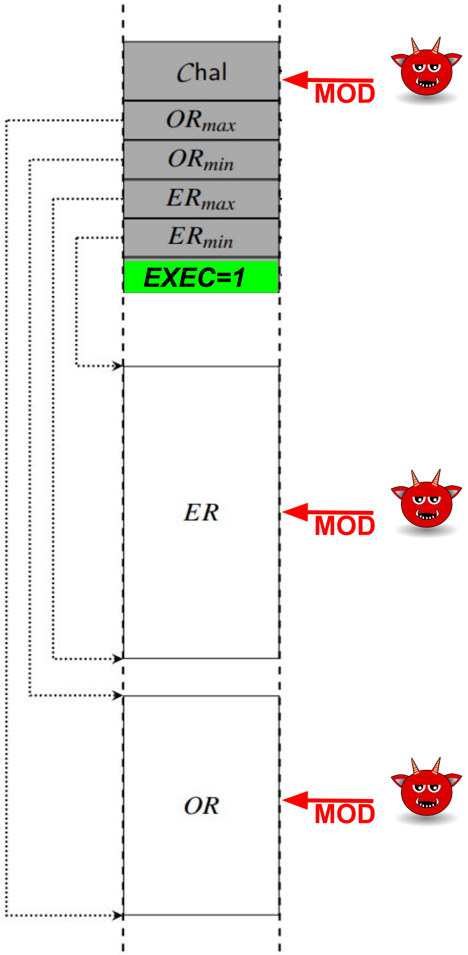
    - Modify METADATA to spoof challenge:
      - Use this execution proof with future challenges (execution replay attack!)

Attested Memory



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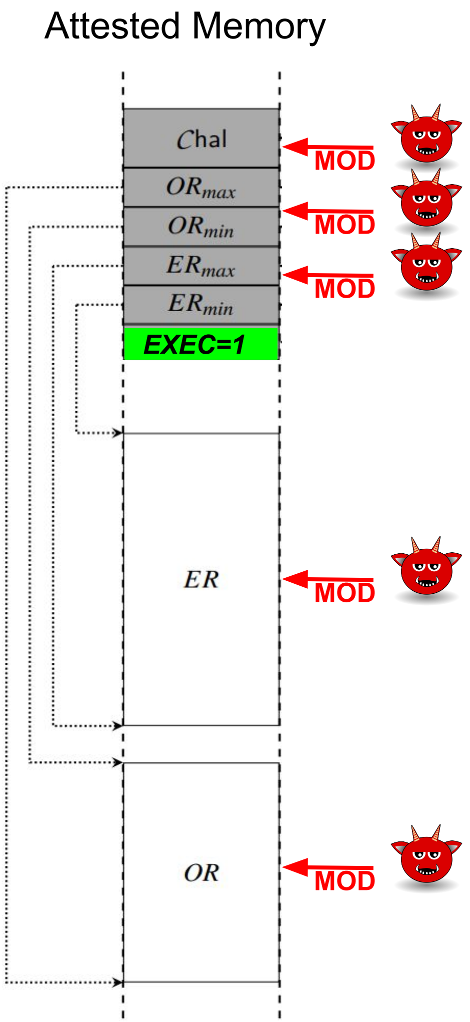
    - Modify METADATA to change ER/OR addresses:
      - Make it look like a valid proof of execution of some other ER, somewhere else in memory.
      - Make it look like this execution produced some other result, stored somewhere else in memory.



APEX Design

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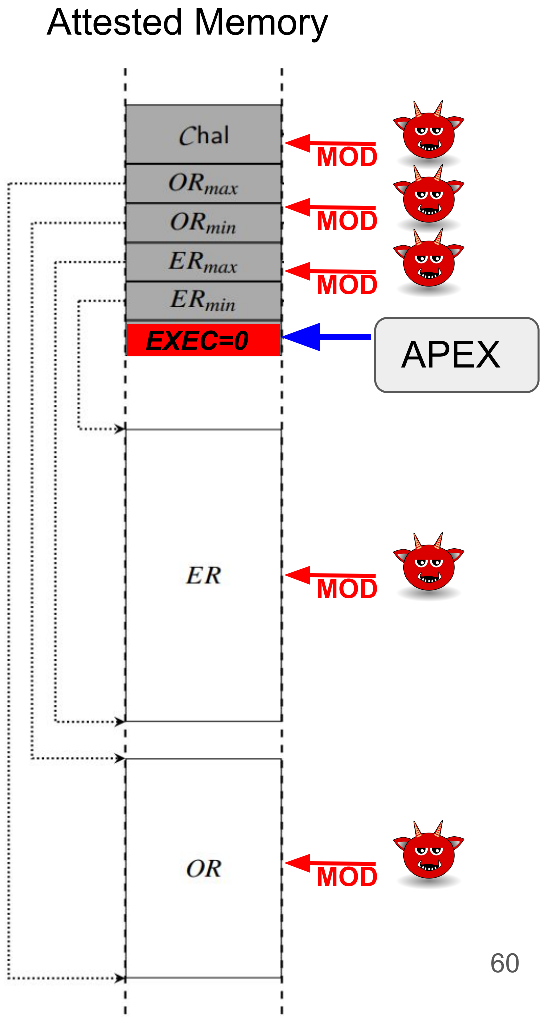
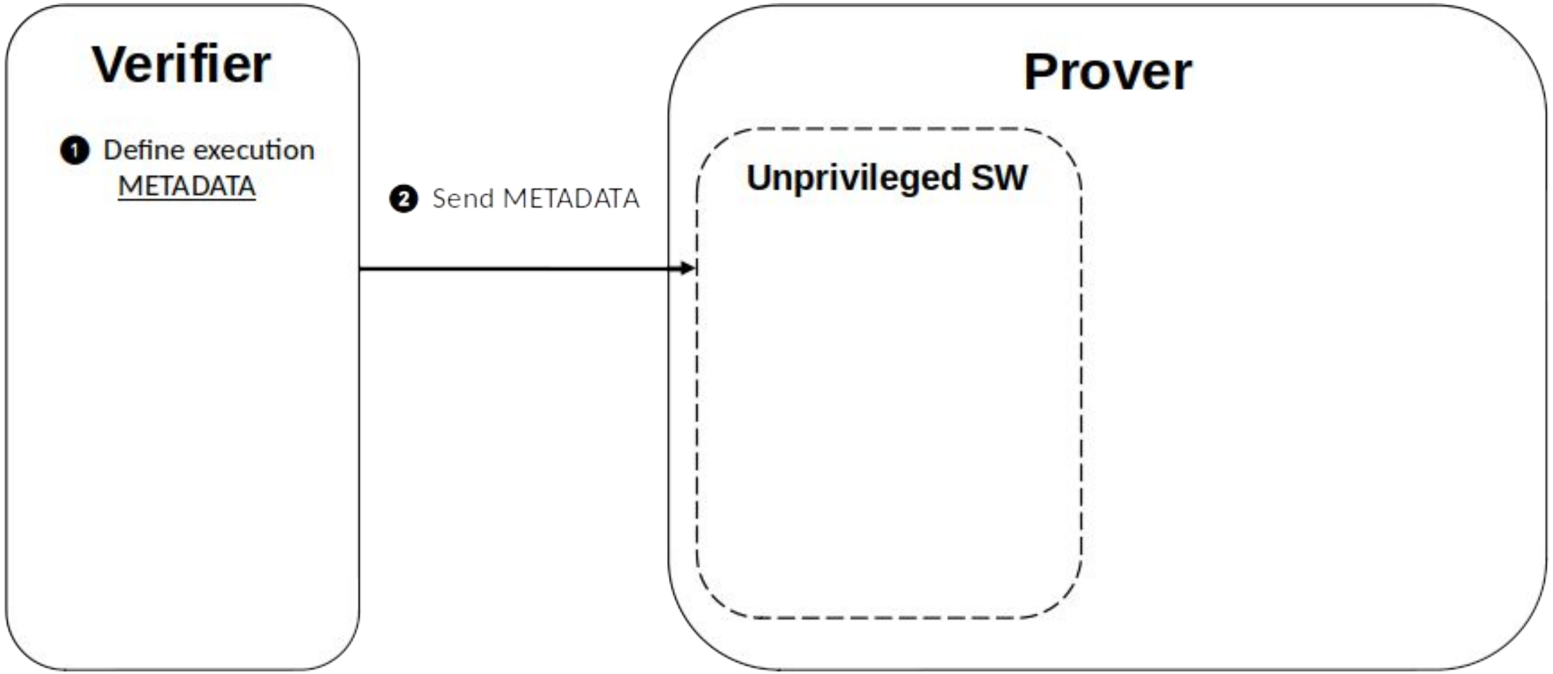
APEX hardware module monitors for such actions setting `EXEC=0` if any of them happen!

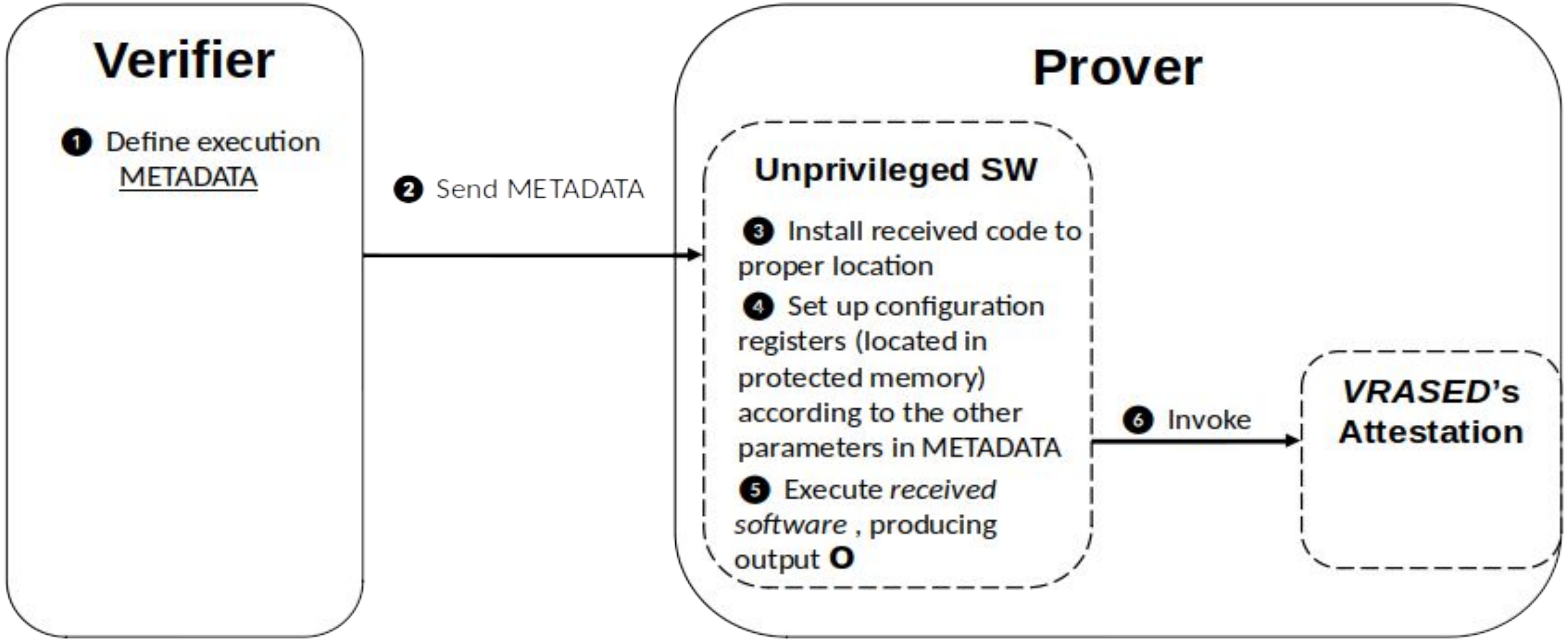


APEX Interaction Summary



METADATA is received by untrusted software running on the Prover that may (or may not):

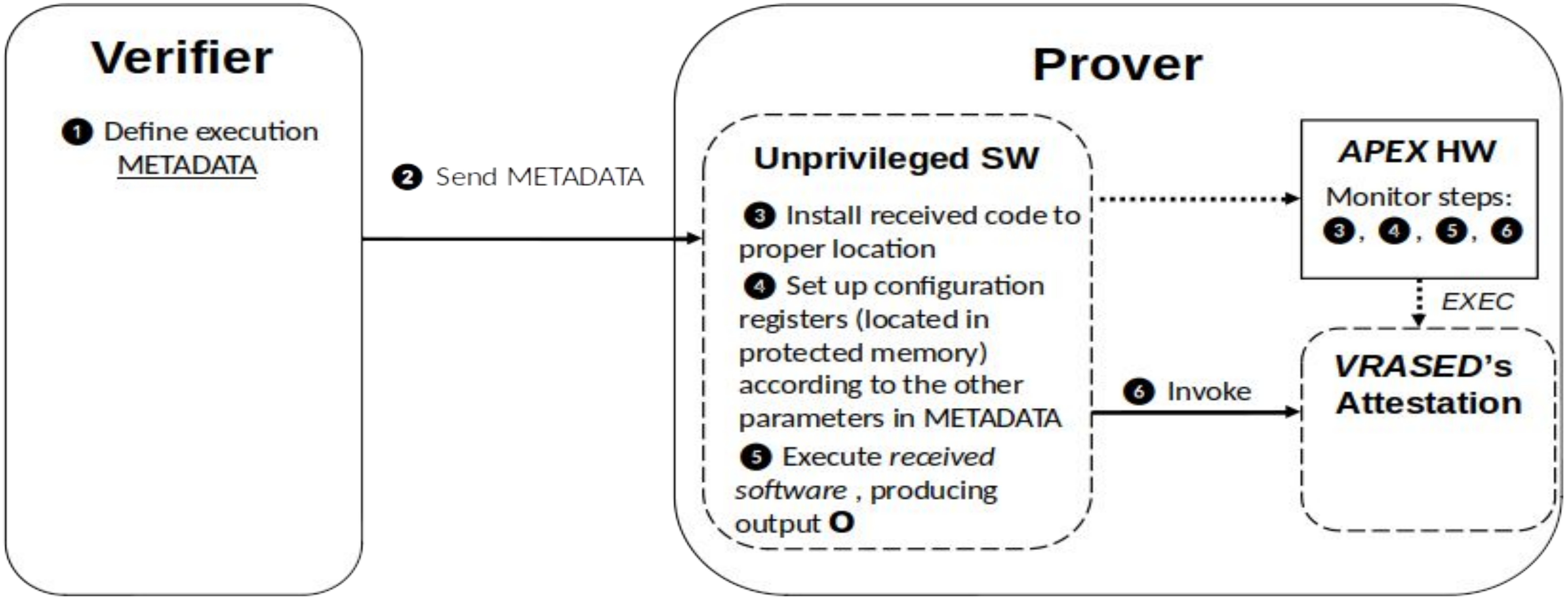
APEX Interaction Summary


Verifier
❶ Define execution METADATA
❷ Send METADATA
Prover
Unprivileged SW
❸ Install received code to proper location
❹ Set up configuration registers (located in protected memory) according to the other parameters in METADATA
❺ Execute *received software* , producing output **O**
❻ Invoke
VRASED's Attestation

METADATA is received by untrusted software running on the Prover that may (or may not):

3. Install the received code in the defined location
4. Setup configuration registers (e.g., "where to store the output" among others)
5. Execute the installed code
6. Call VRASED attestation functionality (locations to be attested defined according to step 4 above).

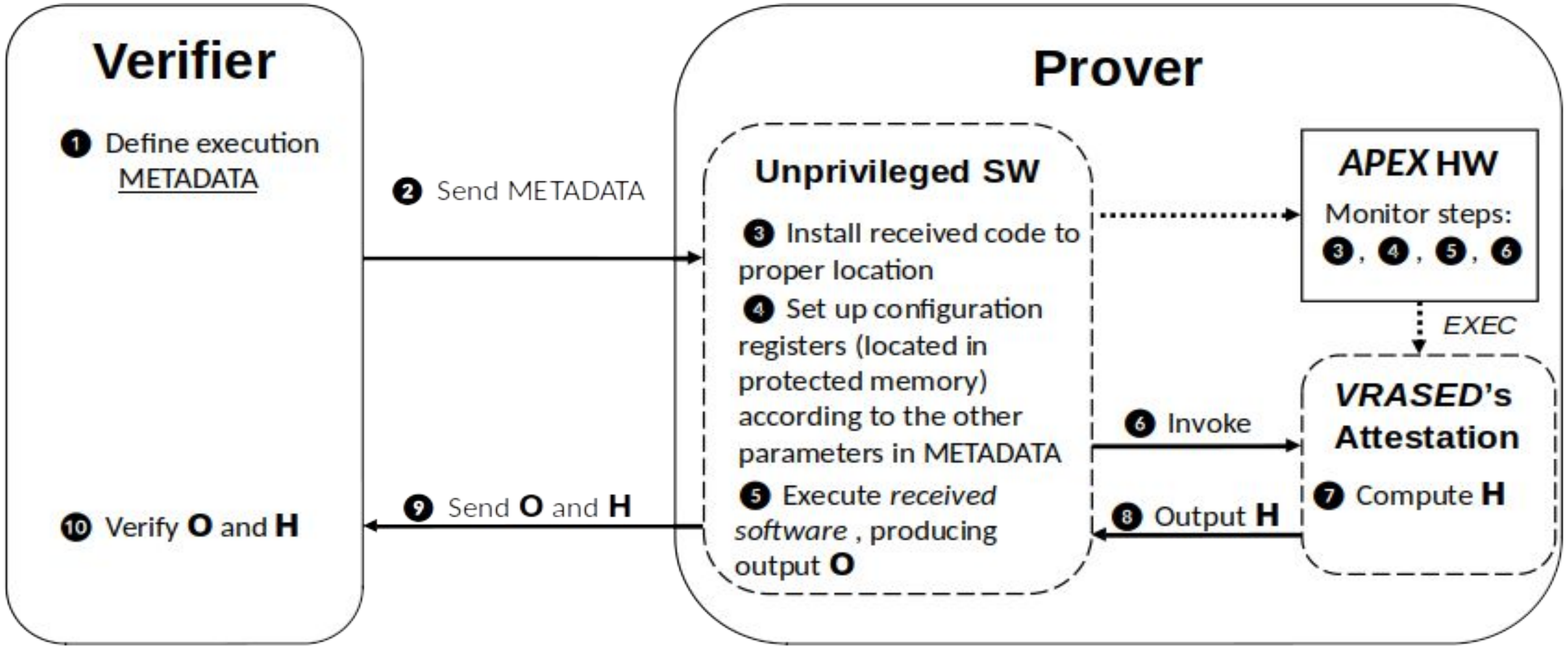
APEX Interaction Summary


Verifier
❶ Define execution METADATA
❷ Send METADATA
Prover
Unprivileged SW
❸ Install received code to proper location
❹ Set up configuration registers (located in protected memory) according to the other parameters in METADATA
❺ Execute *received software* , producing output **O**
APEX HW
Monitor steps: ❸, ❹, ❺, ❻
EXEC
❻ Invoke
VRASED's Attestation

Meanwhile APEX verified hardware monitors steps 3 to 6:

- Controls the value of a 1-bit flag "EXEC".
  - IMPORTANT: EXEC is read-only to all software.
- EXEC=1 if and only if steps steps 3 to 6 happen securely:
  - If untrusted software misbehaves in 3 to 6: EXEC=0.
  - Several important details to the meaning of "securely" omitted in this presentation.
- EXEC value and the execution output are also covered by VRASED's attestation (in addition to the executed code).

APEX Interaction Summary


Verifier
❶ Define execution METADATA
❿ Verify O and H
❷ Send METADATA
❾ Send O and H
Prover
Unprivileged SW
❸ Install received code to proper location
❹ Set up configuration registers (located in protected memory) according to the other parameters in METADATA
❺ Execute received software, producing output O
APEX HW
Monitor steps: ❸, ❹, ❺, ❻
EXEC
VRASED's Attestation
❼ Compute H
❻ Invoke
❽ Output H

<u>VRASED's Attestation produces result H:</u>

- Attestation result **H** is sent back to the Verifier along with output **O**.
- Both "EXEC" flag and are **O** are covered by VRASED's attestation.
- **<u>Verifier will only accept H reflecting EXEC=1.</u>**
- Therefore, Prover can not produce pair **(H, O)** that will be accepted by the verifier unless:

  <u>**O** was indeed produced by the execution expected software (as defined in METADATA).</u>

  Cryptographic challenge ensure freshness of the execution (i.e., no replay of previous executions/results).

APEX Verification

APEX Verification

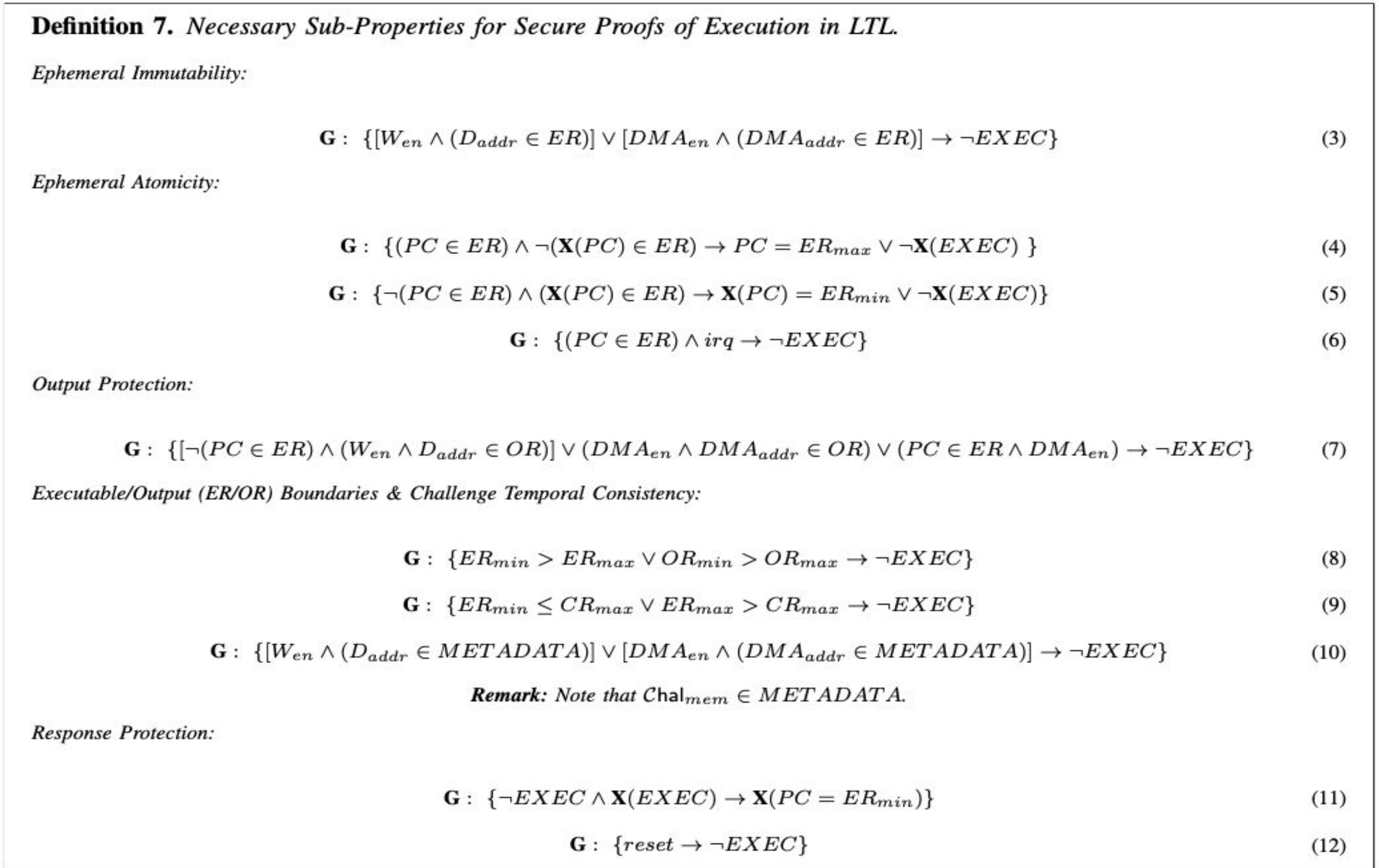
- Formal Verification: Why bother?
  - Formal specification:
    - Provides unambiguous logical expressions to state APEX sub-properties avoiding misinterpretation of requirements.
  - Did we get it right?
    - Once properties are formally specified, the hardware design can be proved to adhere to such properties (computer aided verification via model checking)
  - Are these properties enough?
    - Many properties... we could be missing something!
    - Can use theorem proving to **show that the conjunction of all properties**, when applied to the low-end device machine model **implies an end-to-end notion of secure PoX**.

APEX Sub-Properties Formally

Formalized using Linear Temporal Logic(LTL)

Hardware compliance verified using NuSMV

Check APEX paper for details



Definition 7. *Necessary Sub-Properties for Secure Proofs of Execution in LTL.*

Ephemeral Immutability:

$$\mathbf{G}: \{[W_{en} \land (D_{addr} \in ER)] \lor [DMA_{en} \land (DMA_{addr} \in ER)] \rightarrow \neg EXEC\} \tag{3}$$

Ephemeral Atomicity:

$$\mathbf{G}: \{(PC \in ER) \land \neg(\mathbf{X}(PC) \in ER) \rightarrow PC = ER_{max} \lor \neg \mathbf{X}(EXEC)\ \} \tag{4}$$

$$\mathbf{G}: \{\neg(PC \in ER) \land (\mathbf{X}(PC) \in ER) \rightarrow \mathbf{X}(PC) = ER_{min} \lor \neg \mathbf{X}(EXEC)\} \tag{5}$$

$$\mathbf{G}: \{(PC \in ER) \land irq \rightarrow \neg EXEC\} \tag{6}$$

Output Protection:

$$\mathbf{G}: \{[\neg(PC \in ER) \land (W_{en} \land D_{addr} \in OR)] \lor (DMA_{en} \land DMA_{addr} \in OR) \lor (PC \in ER \land DMA_{en}) \rightarrow \neg EXEC\} \tag{7}$$

Executable/Output (ER/OR) Boundaries & Challenge Temporal Consistency:

$$\mathbf{G}: \{ER_{min} > ER_{max} \lor OR_{min} > OR_{max} \rightarrow \neg EXEC\} \tag{8}$$

$$\mathbf{G}: \{ER_{min} \leq CR_{max} \lor ER_{max} > CR_{max} \rightarrow \neg EXEC\} \tag{9}$$

$$\mathbf{G}: \{[W_{en} \land (D_{addr} \in METADATA)] \lor [DMA_{en} \land (DMA_{addr} \in METADATA)] \rightarrow \neg EXEC\} \tag{10}$$

Remark: *Note that* $\mathsf{Chal}_{mem} \in METADATA$.

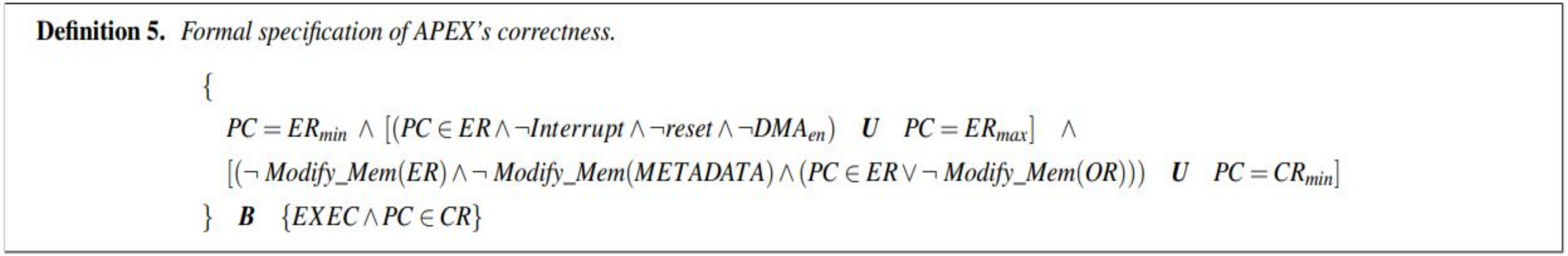
Response Protection:

$$\mathbf{G}: \{\neg EXEC \land \mathbf{X}(EXEC) \rightarrow \mathbf{X}(PC = ER_{min})\} \tag{11}$$

$$\mathbf{G}: \{reset \rightarrow \neg EXEC\} \tag{12}$$

Are APEX Properties Enough?

- The conjunction of APEX properties are shown to imply the following LTL Statement:



Definition 5. *Formal specification of APEX's correctness.*

$$
\begin{aligned}
&\{ \\
&\quad PC = ER_{min} \wedge [(PC \in ER \wedge \neg Interrupt \wedge \neg reset \wedge \neg DMA_{en}) \quad \mathbf{U} \quad PC = ER_{max}] \quad \wedge \\
&\quad [(\neg\, Modify\_Mem(ER) \wedge \neg\, Modify\_Mem(METADATA) \wedge (PC \in ER \vee \neg\, Modify\_Mem(OR))) \quad \mathbf{U} \quad PC = CR_{min}] \\
&\} \quad \mathbf{B} \quad \{EXEC \wedge PC \in CR\}
\end{aligned}
$$

- The notion of **Secure PoX** is formalized as a Security Game
- APEX is hardware is composed into VRASED formally verified RA architecture [Sec'19]
- The composition is shown to imply **Secure PoX**, as long as

  1- VRASED is a secure RA Architecture (RA Security Game), and

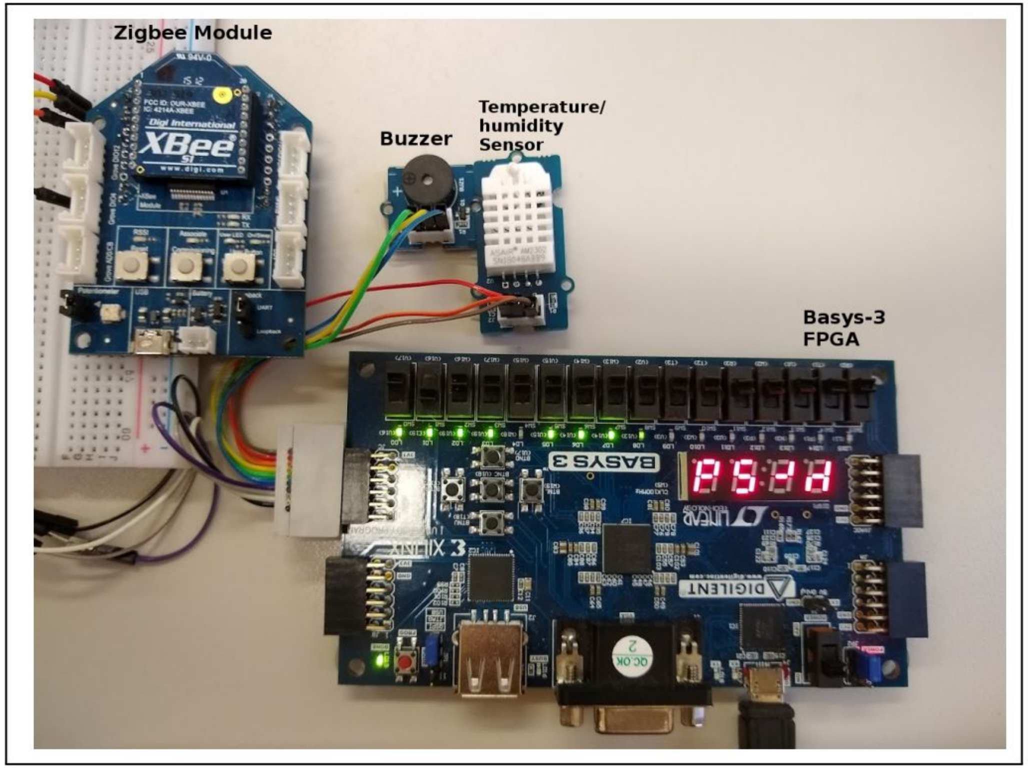
  2- The above LTL statement holds.

See APEX paper for formal definitions and proof details.

Implementation and Evaluation

Implementation and Evaluation

- APEX was instantiated along with VRASED on OpenMSP430 Verilog Design
- Synthesized on Basys3 FPGA
- Used to implement a fire sensor that “cannot lie”.



Publicly Available at:

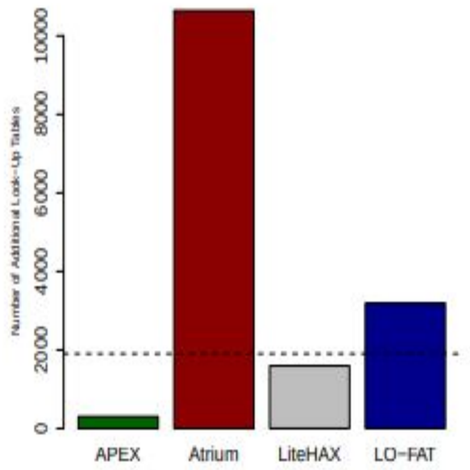
https://github.com/sprout-uci/APEX

Implementation and Evaluation

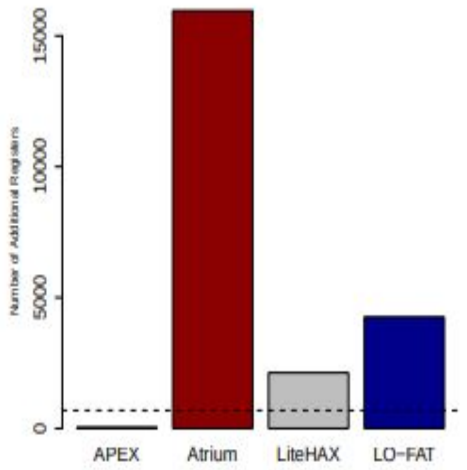
- On top of VRASED:

- 12% more Look-Up Tables
- 2% additional registers

- Relatively inexpensive in comparison with related security services for run-time attestation, such as Control Flow Attestation (CFA).



(a) % extra HW overhead: # Look-Up Tables



(b) % extra HW overhead: # Registers

Thank you for listening.
Questions?