RoCE BALBOA: Service-Enhanced RDMA Offload Engine for Data Center SmartNICs

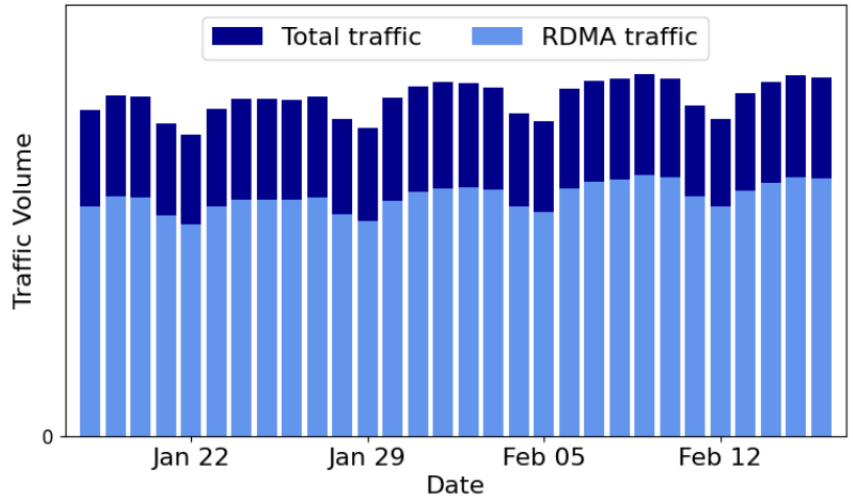
Maximilian Jakob Heer, Benjamin Ramhorst, Yu Zhu,
Luhao Liu, Zhiyi Hu, Jonas Dann, Gustavo Alonso

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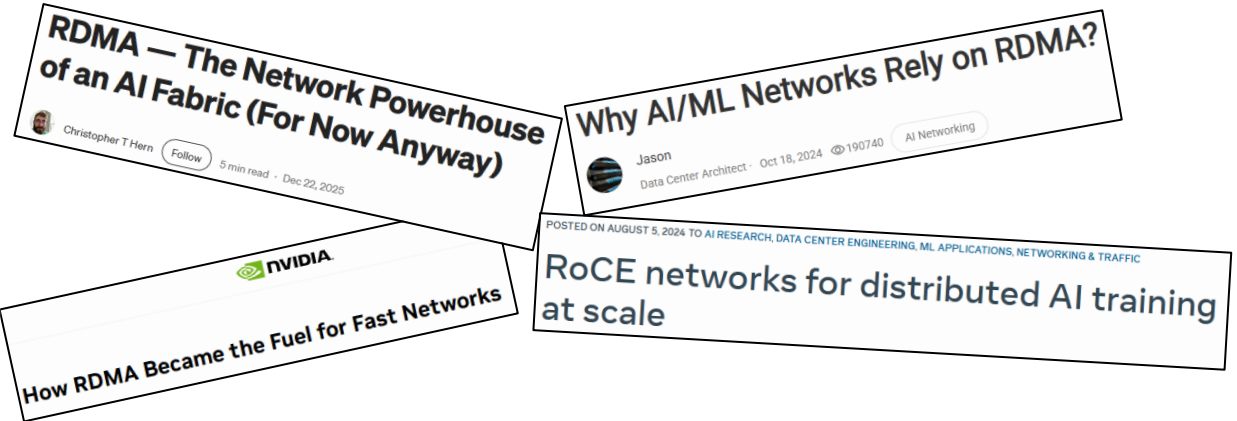


Why RDMA matters…

RDMA is fast, bypasses the OS and is ressource-efficient…



Bai et al: *„Empowering Azure Storage with RDMA“*



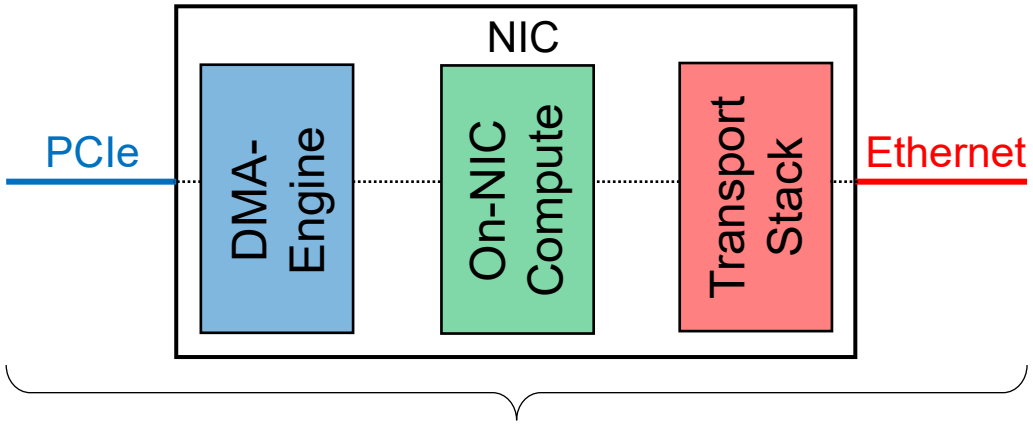
…because it offloads the transport stack to the NIC – *where you can‘t play with it!*

NVIDIA BlueField 3 / 4



AMD Pensando





Hardened, inflexible, with limited interfaces

… and how RoCE BALBOA makes it open for research

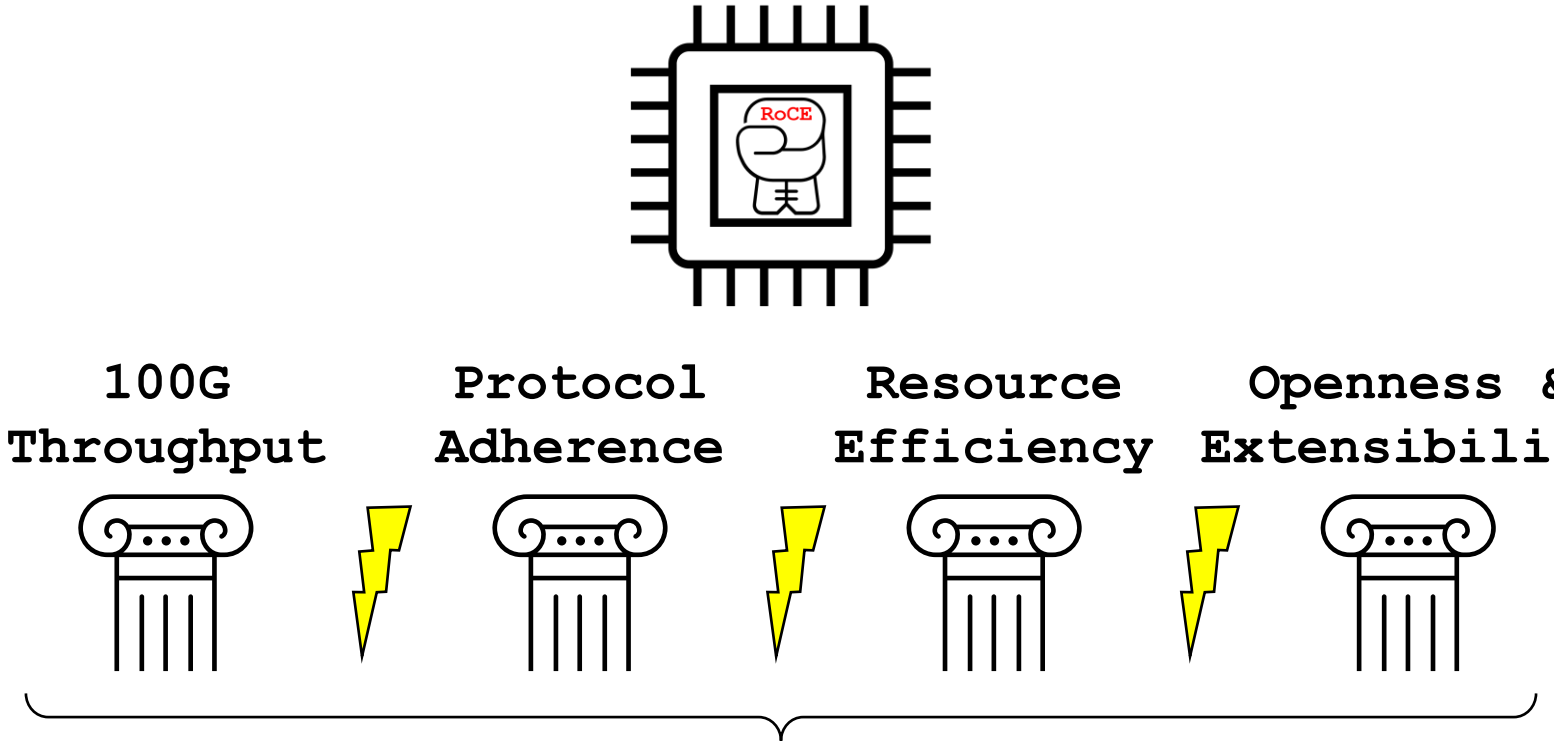
RoCE BALBOA: An open-source core for RoCE v2 networking, i.e. on FPGAs

Embedded in **Coyote v2**

Coyote

Ramhorst et al., SOSP 2025

FPGA-shell for local & network acceleration.



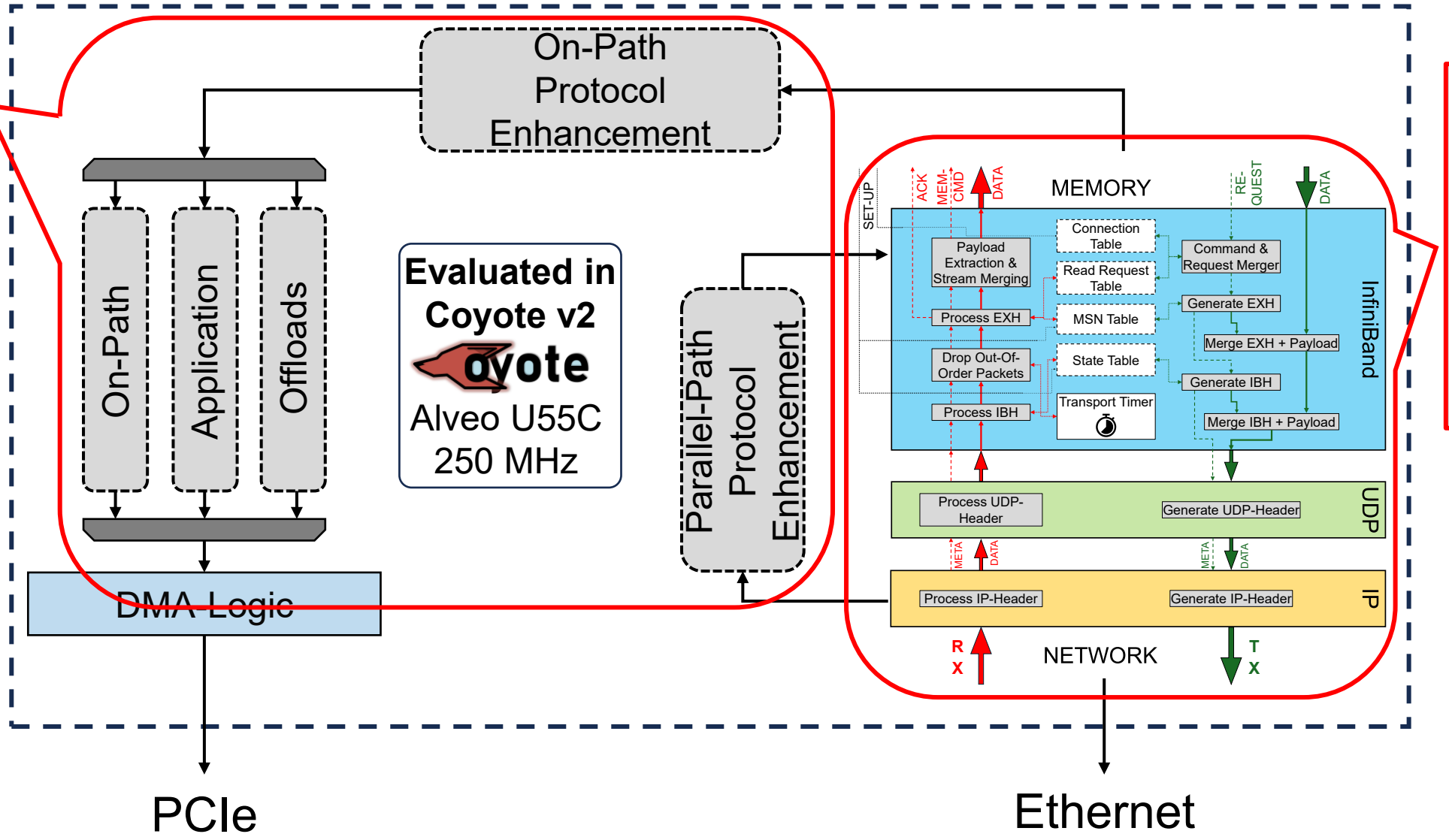
- ✓ **Matches performance** of commercial **100G** RDMA-NICs
- ✓ Is **compatible** with commercial NICs & Switches
- ✓ Designed for **protocol customization & evolution**
- ✓ Allows for **on-datapath acceleration**

Celeris

NIC-offloaded database operators

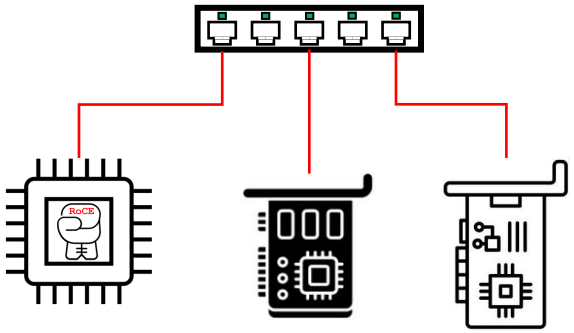
RoCE BALBOA – Architecture Overview

EXTENSION & CUSTOMI-ZATION
On-path / Parallel-path protocol enhance-ments
Routable on-path app offloafs

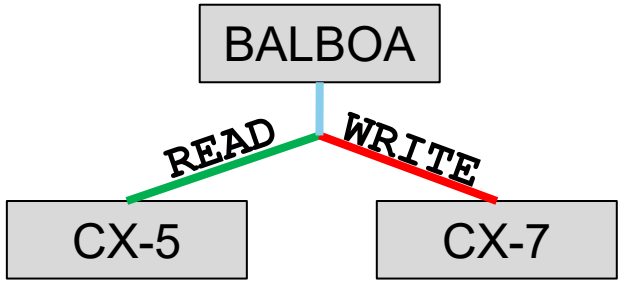


CORE STACK
Packet Processing Pipeline, Flow Control, Retrans-mission

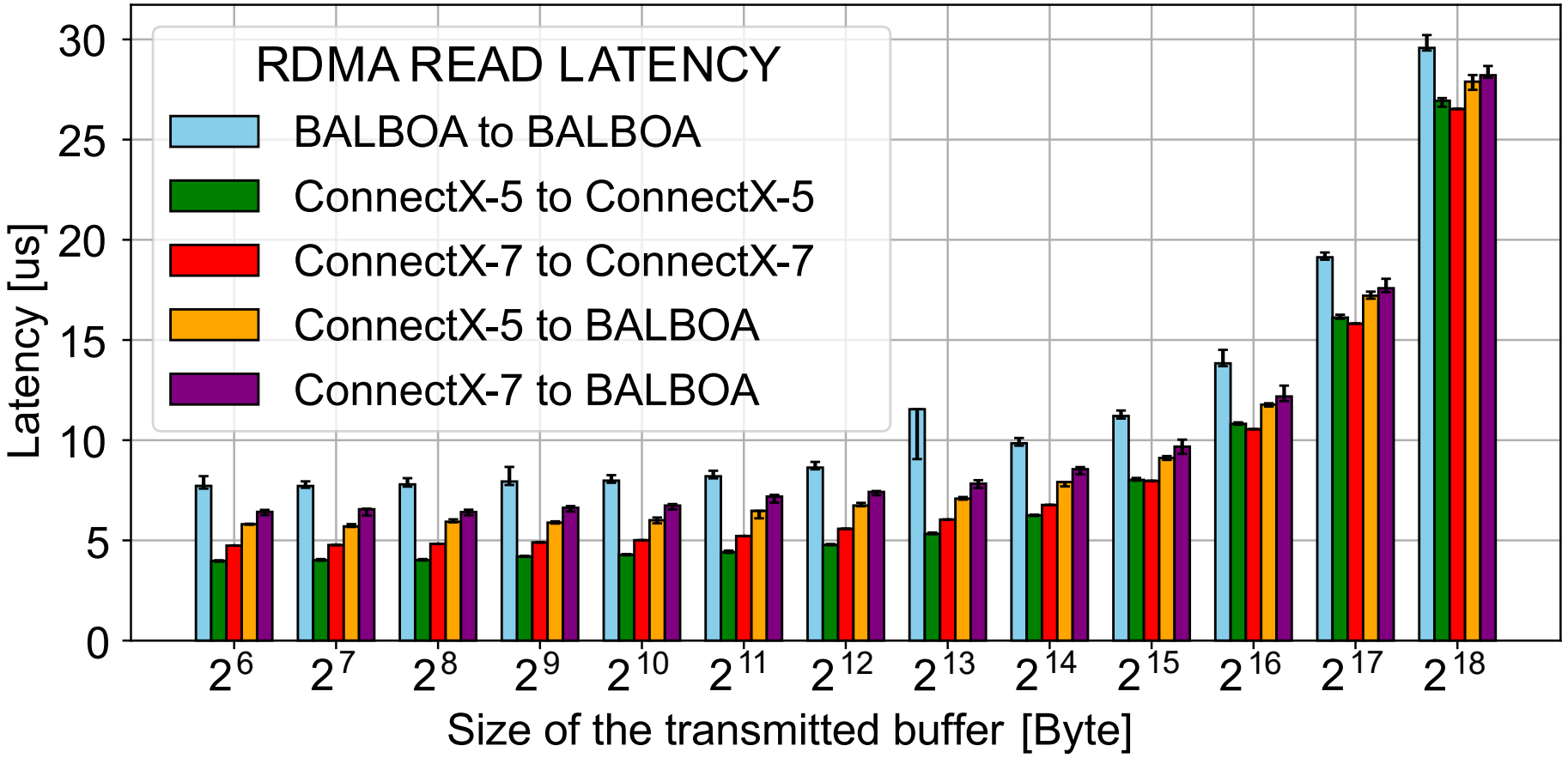
Performance at the core: Throughput & Latency



Tested across a 100G switched connection in the public ETH-HACC cluster



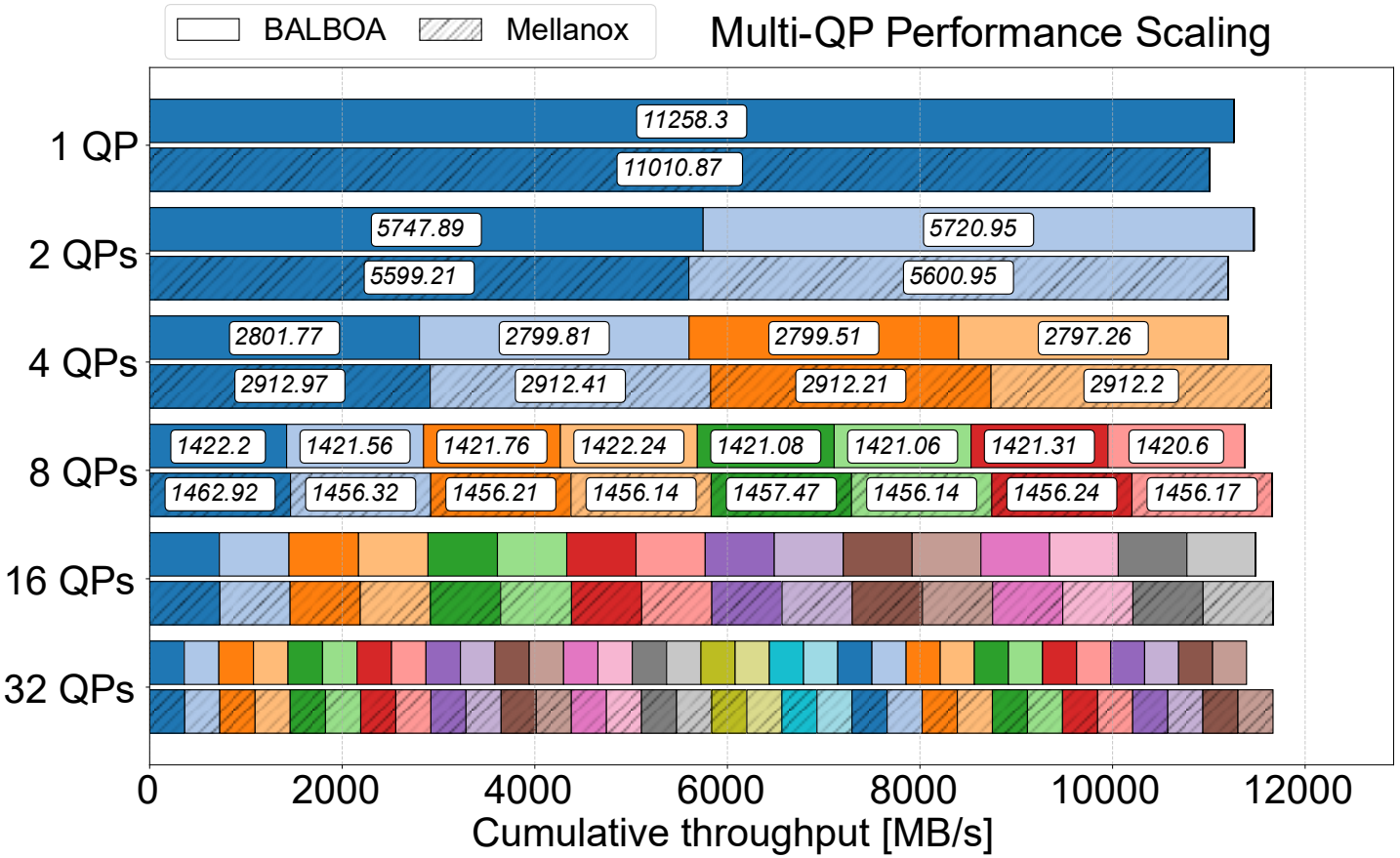
Tested with uni-directional RDMA READ / WRITE bulk transfers



CONCLUSIONS:

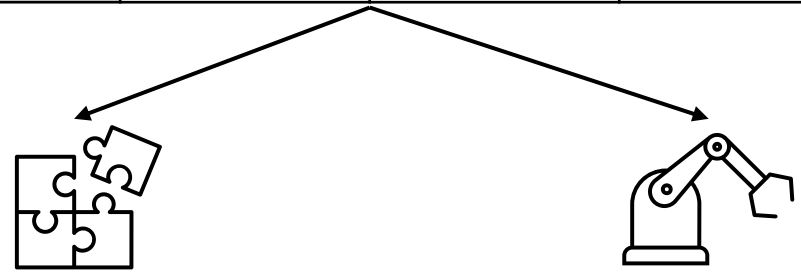
- Disadvantages at latency & small message throughput due to raw clockspeed
- KEY: Full saturation at 100G bandwidth

To the stars & beyond: Scalability



Resource Utilization on an Alveo U55C FPGA:

	LUTs	BRAM	FFs
BALBOA	3.4%	5.1%	4%
Limago (TCP)	4.2%	3.93%	2.83%



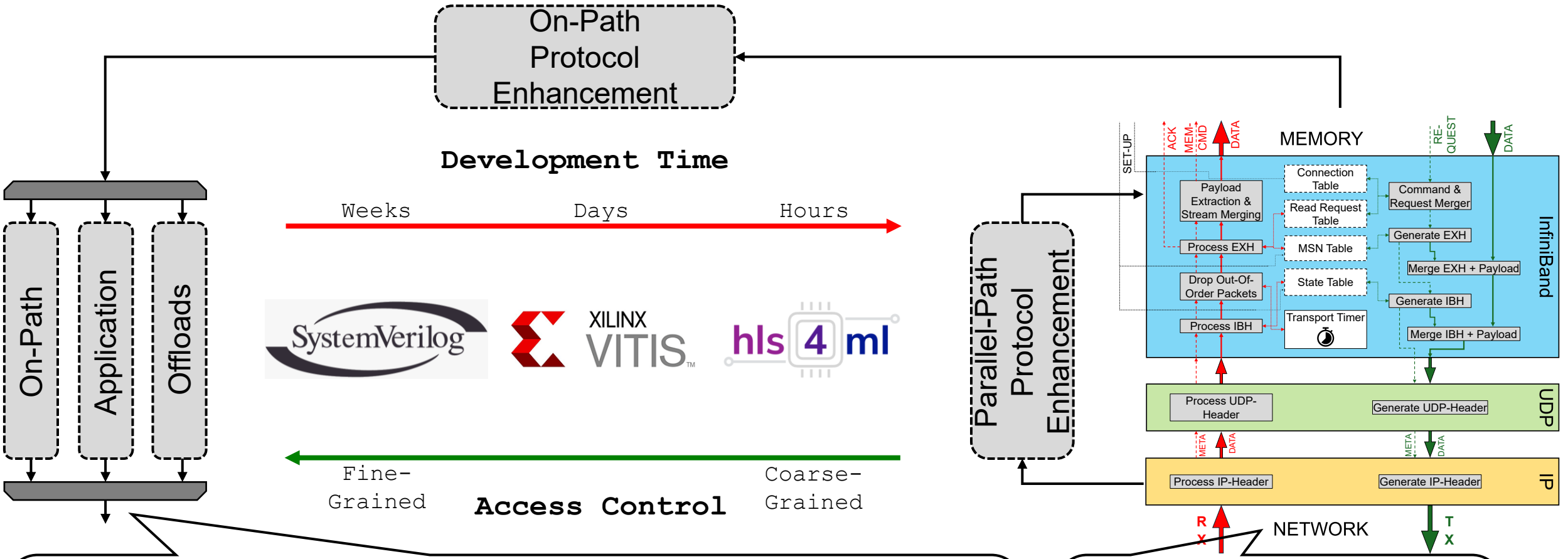
Leaves Space for offloads & enhancements

Can be adopted for robotics & embedded AI

Data Center Usability:
Native support for hundreds of QPs without performance lass through efficient scheduling.

Resource Efficiency:
Allows for collocation with offloads & adaptation to embedded platforms

Extensibility as design principle



Development Tools for Offloads

Plug & Play through AXI

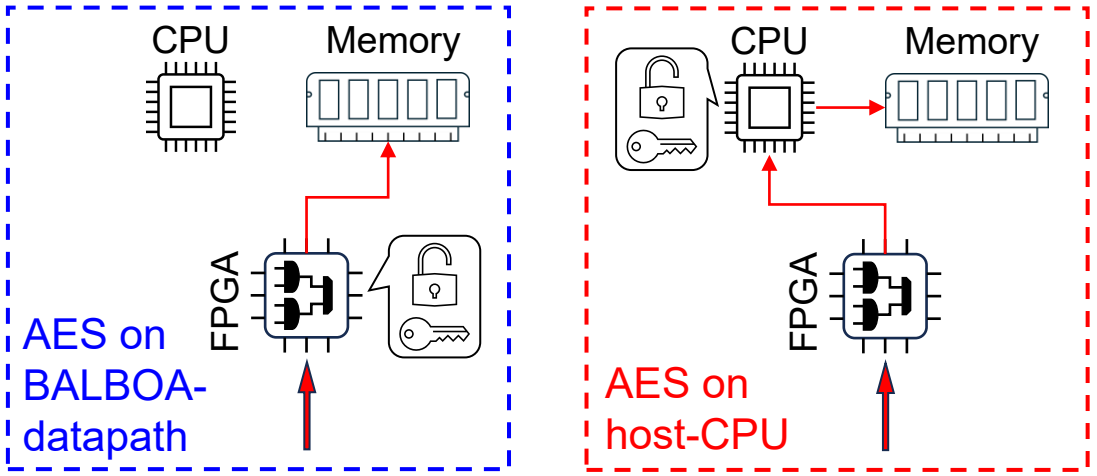
Statefulness through Ctrl-Regs

Simulation Suite

Designed for Extensibility

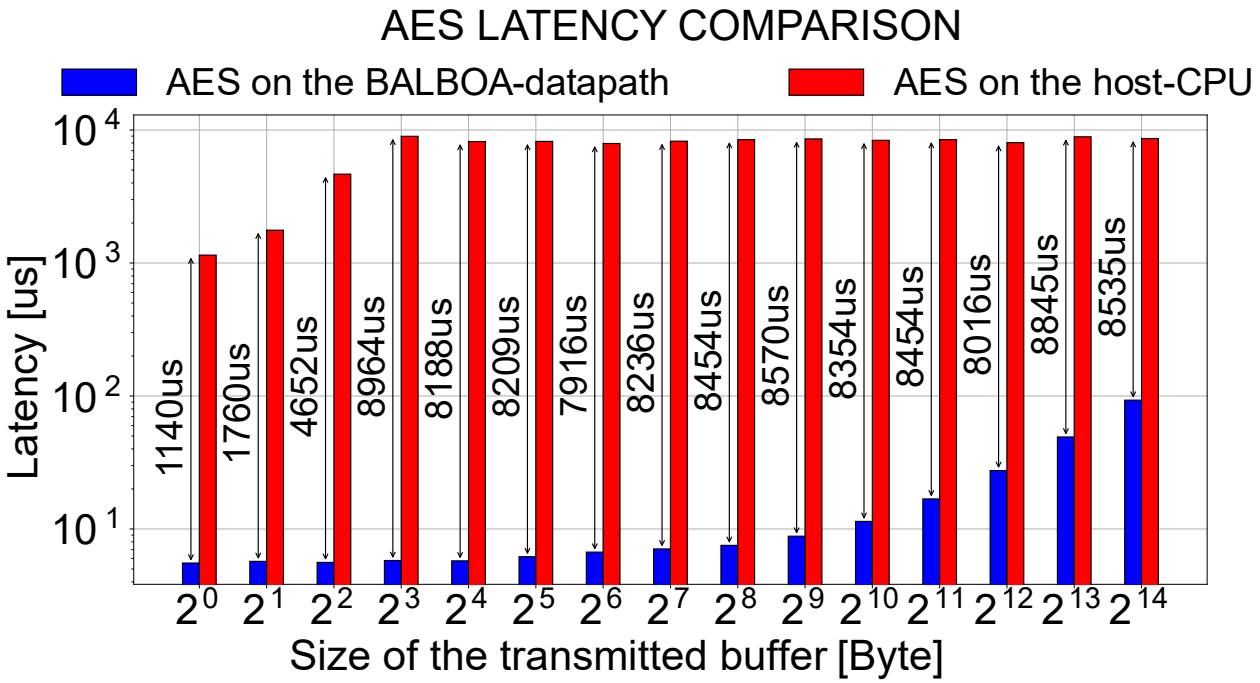
Functional Encapsulation

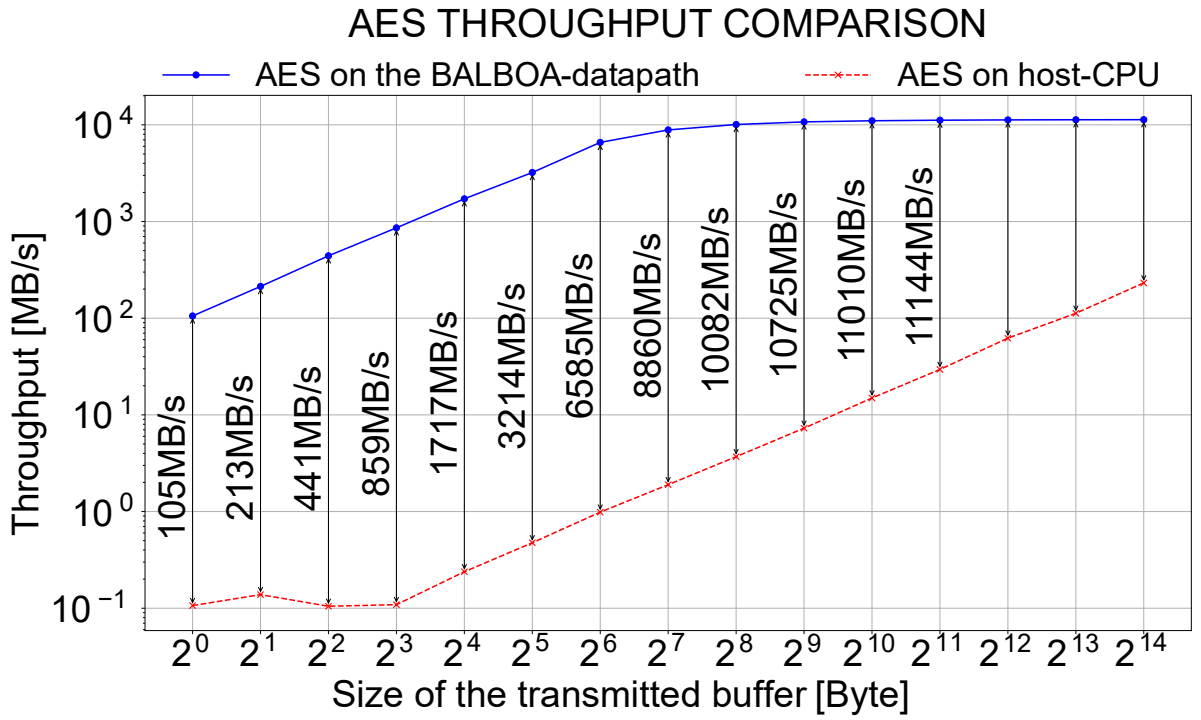
On-path protocol enhancements: AES CTR



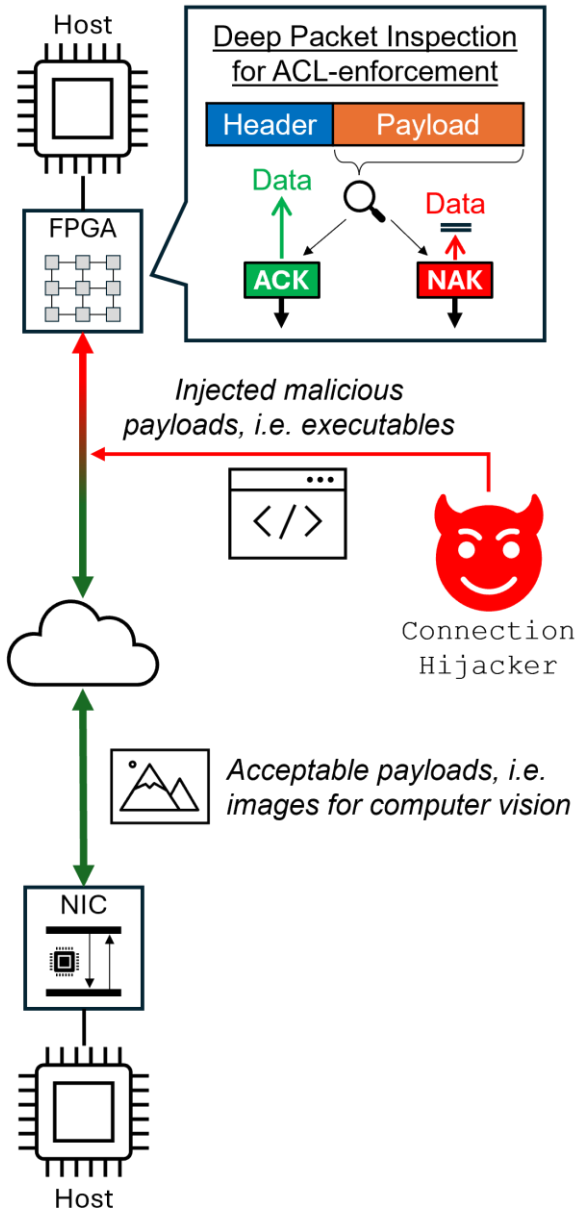
Main advantages of placing logic on-datapath on FPGA-NICs:

- Stream computation at full throughput / line rate
- Automatic workload scheduling without synchronization overhead



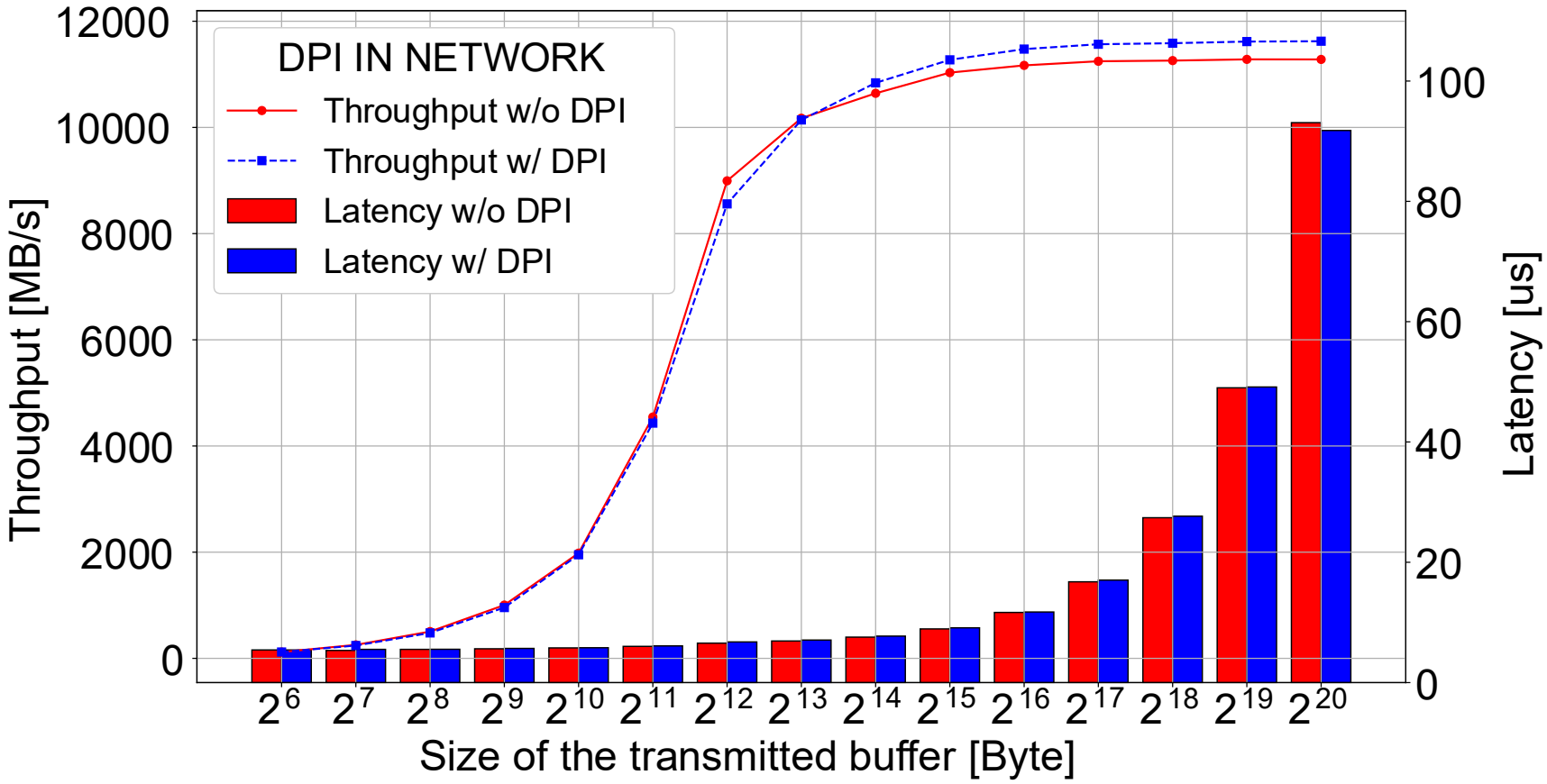


Off-path protocol enhancements: ML DPI

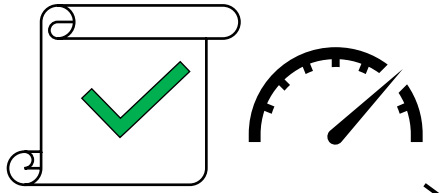


ML-based Deep Packet Inspection with HLS4ML on FPGAs:

- Differentiate between **malicious executables** and **acceptable payloads**
- Unique for BALBOA: **Direct impact on the protocol stack**
- Achieving **100G** line rate with **98% accuracy**



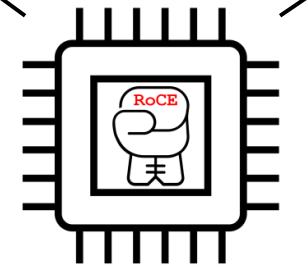
RoCE BALBOA – a summary



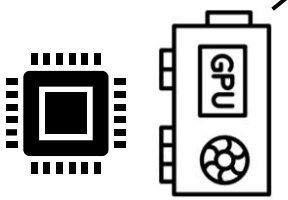
RoCE-compatible, works with switches, 100G line rate



Fully customizable & extendable



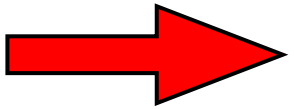
RoCE BALBOA



Works with heterogeneous hardware



Fully opensourced



Check out BALBOA & our open-source FPGA ecosystem!

