

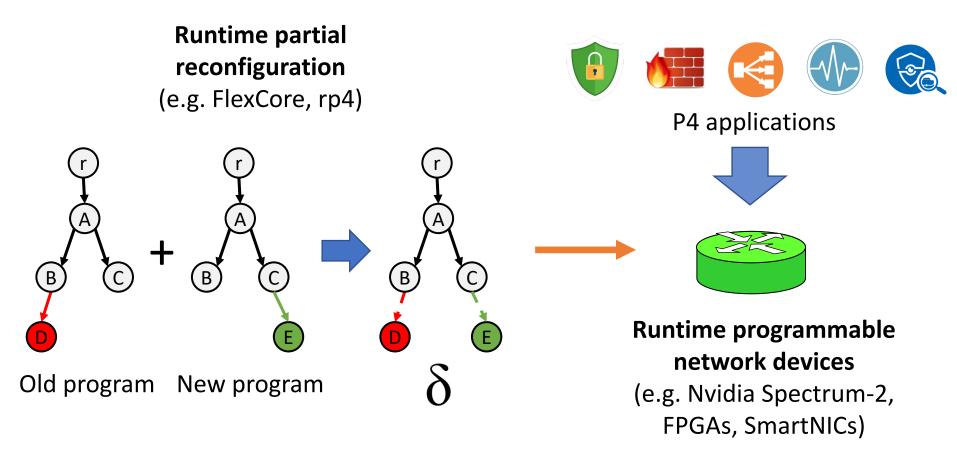


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# FlexPlan: Synthesizing Runtime Programmable Switch Updates

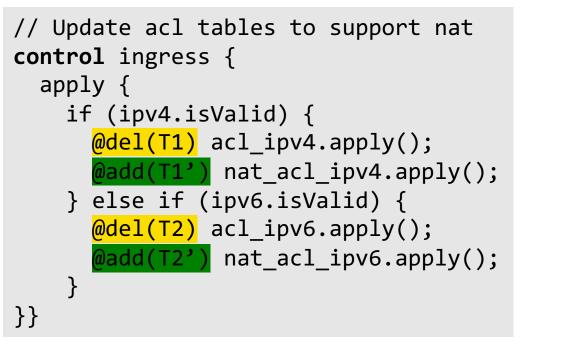
Yiming Qiu, Ryan Beckett, Ang Chen

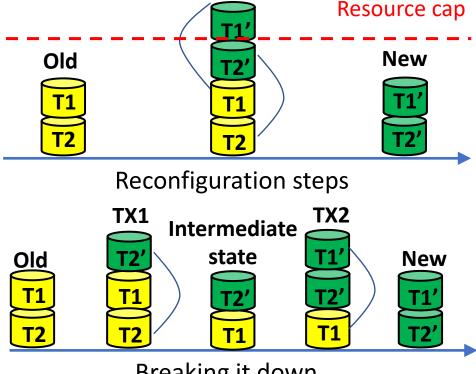
# Background: Runtime programmable devices



- Capable of runtime reconfiguration with **zero downtime** 
  - FlexCore (NSDI'22) based on Nvidia Spectrum-2 switches
  - rP4 (NSDI'22) based on Xilinx Alevo FPGAs

# Background: multi-step runtime update



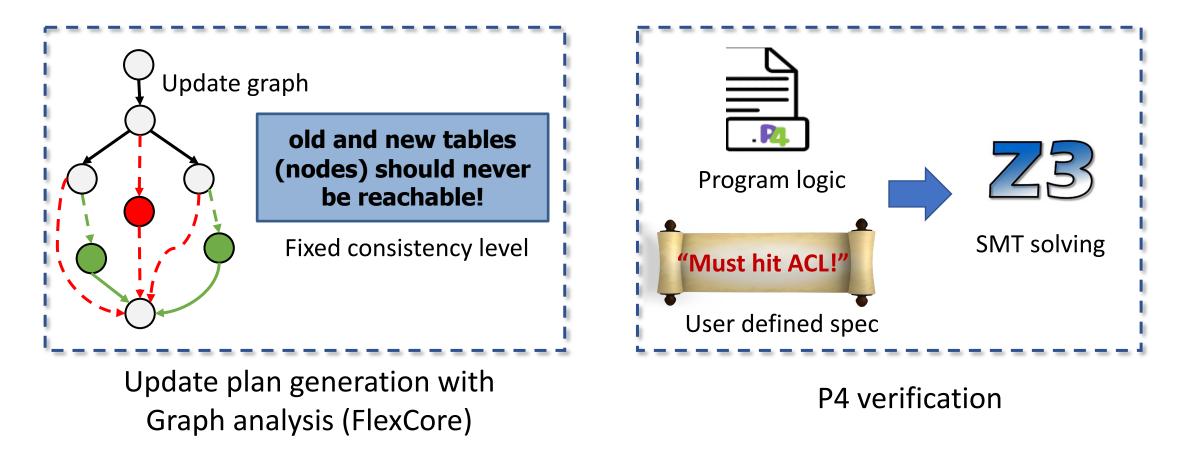


P4 program update

Breaking it down

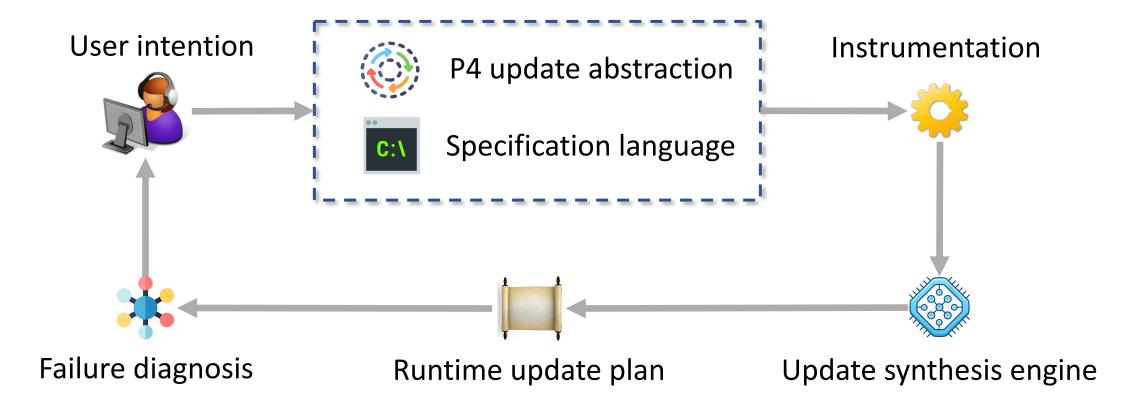
- Updating everything all at once not always feasible
  - Update transaction (TX) could cause significant resource spike
  - Multi-step update possible, but causes intermediate states
- Regulate intermediate states with consistency guarantees!

# SOTA: graph analysis and P4 verification



- Graph analysis does not support program semantics/user defined specs
- P4 verification does not support update reasoning/task of synthesis

#### FlexPlan: a formal synthesis approach



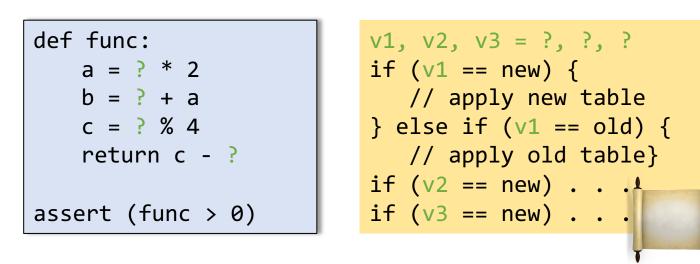
 FlexPlan: a formal approach to generate update plans that are both safe (consistency guarantee) and feasible (resource usage)

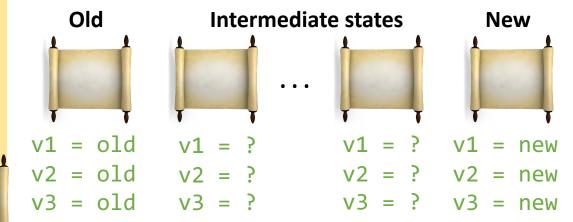
# Specification language

<pre>specification {     // create new ghost variables for the program</pre>	Specifications	LoC
<pre>ghost bit sawOld = false; ghost bit sawNew = false;</pre>	 Execution consistency for IPv4	13
<pre>// update variables when annotations encountered @old =&gt; { sawOld = true; } @new =&gt; { sawNew = true; }</pre>	Field consistency for egress spec	8
	Program consistency for TCP	13
<pre>// define no ipv4 packet mixes old and new logic execution consistency = {</pre>	Element consistency for ACL	15
<pre>\$pkt.ingress.ipv4.isValid() =&gt;     !(\$pkt.egress.sawOld &amp;&amp; \$pkt.egress.sawNew); }</pre>	Table consistency for ECMP	10
	Correct VLAN table access	8
<pre>assert execution_consistency; }</pre>	Correct TTL decrement	6

• Flexible consistency/safety specification based on user intentions

#### Program update sketching





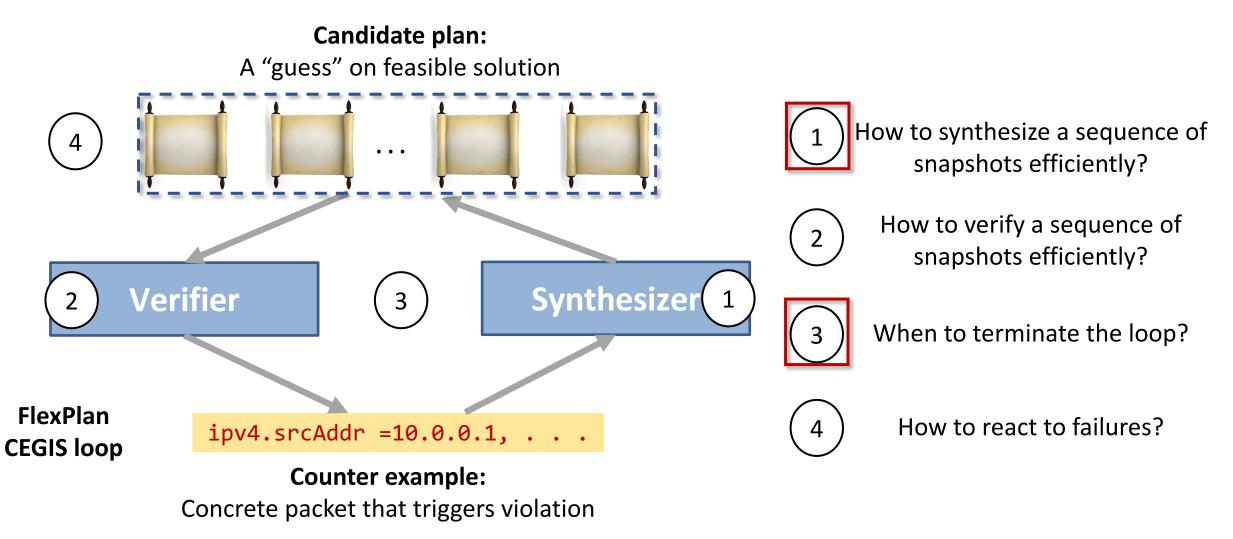
Program sketch [1]: Representing possible programs Version sketch: Representing possible intermediate states Sequence sketch:

Representing possible update plans (sequence of version sketches)

• Translating update plan generation into a sketching problem

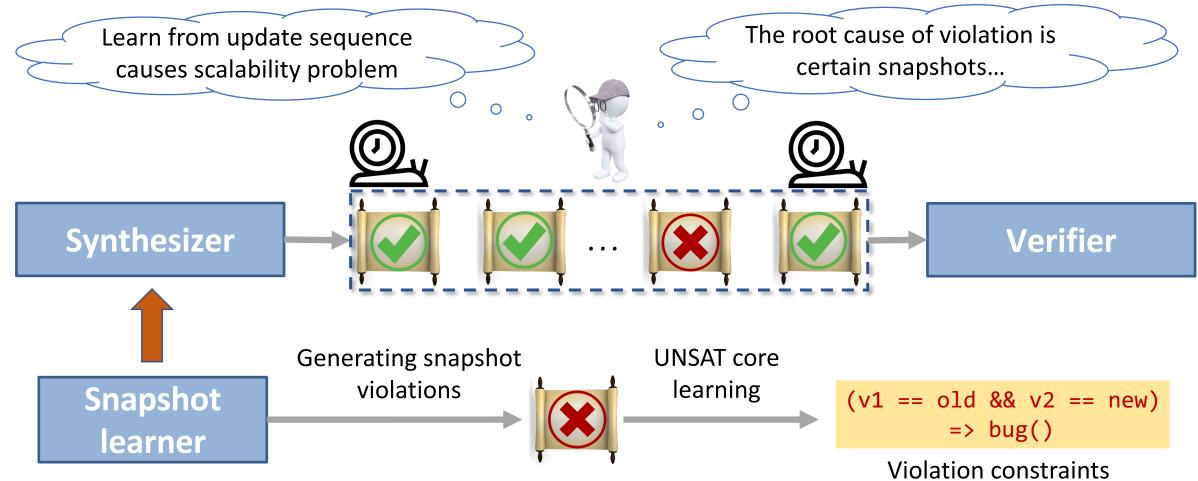
[1] Combinatorial sketching for finite programs. ASPLOS'06

# FlexPlan CEGIS loop



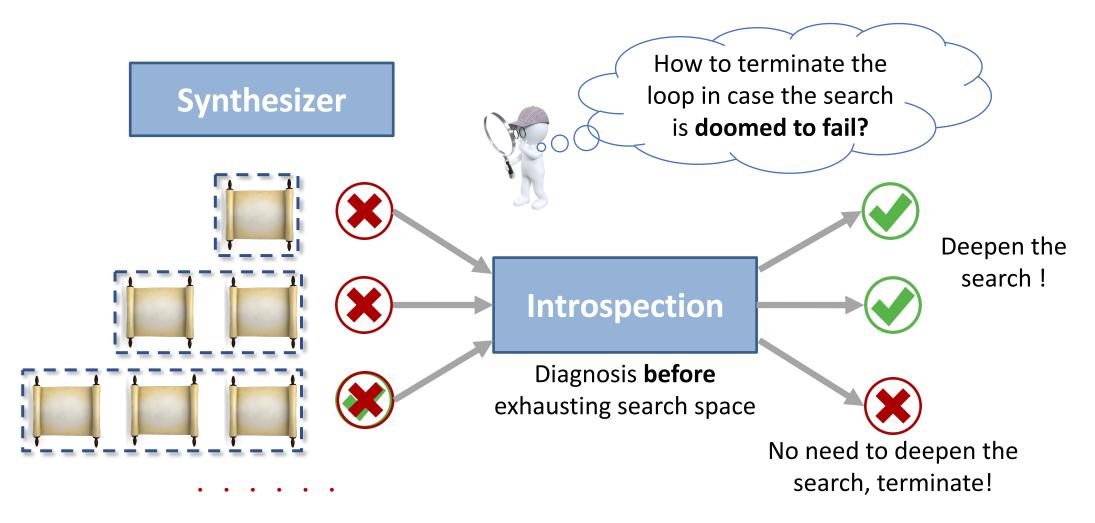
• Counter Example Guided Inductive Synthesis (CEGIS)

# **Optimization:** Snapshot learning



• Learn from single snapshots, not entire sequences

#### **Optimization:** Loop termination

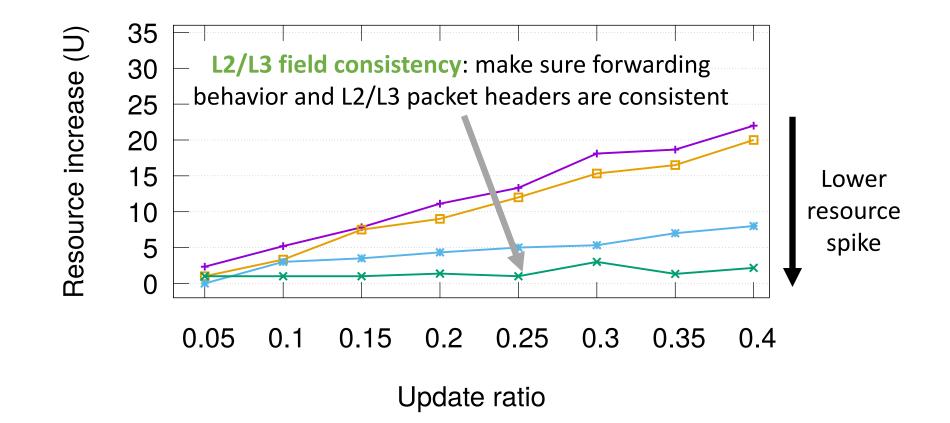


• Novel early termination technique (more in the paper)

#### Implementation and setup

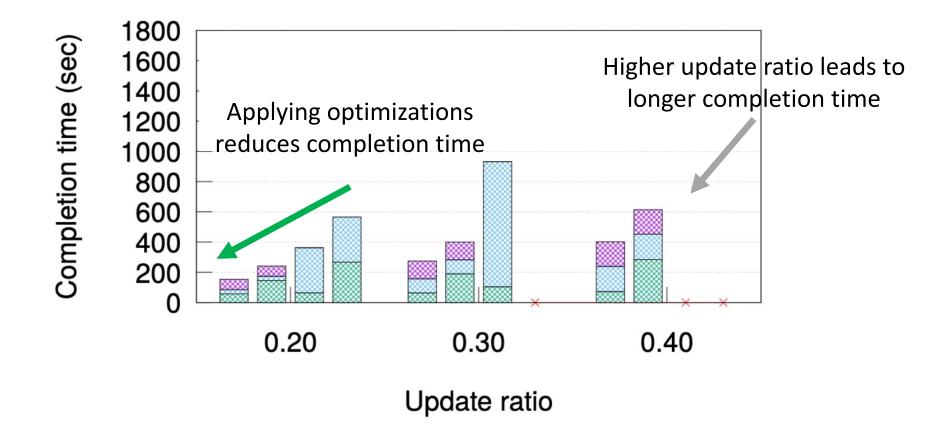
- FlexPlan prototype
  - https://github.com/824728350/FlexPlan
- Case study setup
  - Various P4 programs such as **switch.p4** (~6000LoC)
  - Both random and manually crafted program updates
- Evaluation questions (more in the paper!)
  - Do the specs generate granular update plans?
  - Do optimizations tackle scalability problem?

#### Expressive specs save resources



- FlexPlan supports various user defined consistency levels
- FlexPlan spec language provides significant resource saving

# Optimizations improve scalability



- Higher update ratio results in longer completion time
- Snapshot learning/verification improve scalability significantly

#### Summary

- FlexPlan: a formal approach to generate update plans that are both **safe** (consistency guarantee) and **feasible** (resource usage)
- Hardware agnostic update plan generation framework
- Define your own runtime consistency requirements
- If there is a valid update plan, we'll find it.
- If we find a update plan, then it is correct!

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