

Design of All Programmable Innovation Platform for Software Defined Networking

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1 Introduction

Software Defined Networking (SDN) breaks the barrier of Internet innovation and has attracted tremendous attentions from both industrial and academic communities. Although OpenFlow is the de factor SDN protocol nowadays, which defines the interface between the data plane switches and the control plane controllers, there are emerging SDN proposals. Even for OpenFlow itself, it keeps evolving. As a result, a flexible SDN data plane switch, which is capable to upgrade the processing logic, is highly desired for the research and innovation purpose.

In general, there are three ways to realize SDN/OpenFlow switches in the community. The first way uses software OpenFlow Switches (OFS), *e.g.*, Open vSwitch [2]. Software OFS is easy to deploy and modify, but it is hard to guarantee the performance for wire-speed processing. The second option is the commercial OFS. Commercial OFS provides stable performance and sufficient network interfaces. However, it cannot be modified with innovated processing logic to update with evolving SDN/OpenFlow specifications. Commercial OFS is an SDN-enabled platform for mature applications but not a good SDN-innovation platform for research. NetFPGA, as the third methodology, offers the opportunities for users to change the hardware logic through FPGA [1]. NetFPGA is quite successful for networking research, but it has limitations when using for SDN innovation. The first generation NetFPGA-1G does not provide enough resources for OFS processing, *e.g.* flow tables, meters. And its PCI interface is the bottleneck to offload traffic to host CPU and remote controller. The second generation of NetFPGA-10G supports 10G fiber interface and contains more hardware resources, but there is no stable SDN/OpenFlow reference design for further research.

In this paper, we have designed ONetSwitch, which is an “all programmable” SDN innovation platform with high-performance, low-power, flexibility and the minimized size (7 in* 7 in* 1.75 in). The “all programmable” feature is empowered by the emerging Xilinx Zynq SoC, which makes ONetSwitch software programmable and hardware restructural. We also present an OFS design based ONetSwitch among many research scenarios over ONetSwitch.

2 Design and Building Case of ONetSwitch

The design diagram of ONetSwitch is depicted in Fig. 1. The main chip of ONetSwitch is the Xilinx Zynq-7045 SoC, which integrates ARM Cortex-A9 dual core processor-based processing system (PS) and Kintex-7 FPGA-based the programmable

logic (PL) into a single chip. The PS part makes ONetSwitch software programmable and the PL part enables the reconstruction of the hardware logic. To form ONetSwitch, Zynq PL is connected with four Gigabit Ethernet Media interfaces by a quad-port physical layer interface and four SFP+ 10G interfaces with 10G-Base-KR interfaces. Another physical layer interface is directly connected to Zynq PS, realizing the channel with controller by a copper port for Gigabit Ethernet. Zynq also attaches one QDR II+ SRAM on the PL side and four DDR3 chips on the PS side. One Mini PCI Express card slot is provided, which compatibles with commodity wireless adapter modules to support 802.11 a/g/n. Furthermore, ONetSwitch is hardware extendable with high speed and low speed connectors. An FMC connector can be extended with daughter boards such as 10G Ethernet board, TCAM flow table board. There is also one low speed connector on board to support basic control and low speed data transfer, like GPS, sensors, or other modules. ONetSwitch also provides USB-UART, SD card slot, USB host connector, SIM, debugger ports for FPGA and ARM. Configuration files can be downloaded through JTAG interfaces as well as on board SPI flash and SD card. At last, we would like to mention the power measurement circuit we designed for ONetSwitch, which monitors the total power and core power of the platform.

ONetSwitch is capable of building many research scenarios, *e.g.*, switch, router, OFS, data center network, *etc.* Here we propose a new design of OFS based on ONetSwitch in Fig. 2. The data path of our OFS is a hybrid hardware and software solution. The flow table lookup operation is first triggered in the hardware flow tables with hot entries and the software flow tables with all the table entries are activated only when a lookup misses in hardware. The intelligence on how to divide tables into hardware and software is implemented in Hardware Abstraction Layer (HAL). HAL translates original flow entries from the controller into the semantic-equivalent formats that optimize the OFS performance. The switch management module is used to embed newly proposed or private message format, protocol with (multi-)controller and table management schemes. The rest part of our OFS software design is based on CPqD OpenFlow 1.3 reference software switch. The design in Fig. 2 is also recognized as a framework and people can enable their new designs by replacing the related functional modules.

3 Evaluation

The comparisons between ONetSwitch and NetFPGA on hardware specification is illustrated in table 1. ONetSwitch is a fully upgrade of NetFPGA in hardware arrangement by pro-

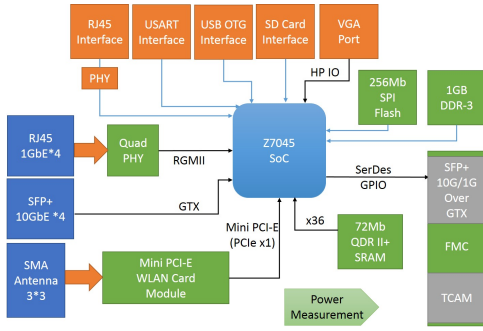


Figure 1: Design diagram of ONetSwitch.

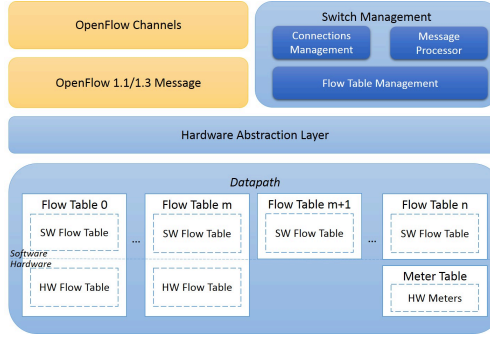


Figure 2: A design of OFS on ONetSwitch.

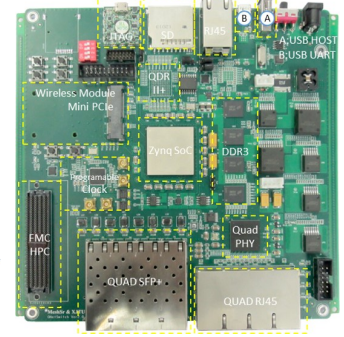


Figure 3: The picture of ONetSwitch

Table 1: Comparisons of Hardware Specification

	NetFPGA 1G	NetFPGA 10G	ONetSwitch
Arch.	Card+Host	Card+Host	Standalone
Logic Cell	53,136	239,616	350,000
Blk. Mem	522KB	1,458KB	2,180KB
Processor	N/A	N/A	800MHz*2
SRAM	4.5MB SRAM	27MB QDR II+	9MB QDR II+
DRAM	64MB DDR2	216MB RLDRAM II	1GB DDR3
Net. I/F	RJ45x4	SFP+x4	SFP+ x4+RJ45 x4
Host I/F	PCI(1Gbps)	PCIEx16 Gen2(40Gbps)	AMBA(100Gbps)

Table 2: Performance Comparison

	SW	NetFPGA	ONetSwitch
HW entry	N/A	32	1K+
SW entry	unlimited	N/A	unlimited
Throughput1	211Mbps	1Gbps	1Gbps
Throughput2	12.8Kpps	1.5Mpps	1.5Mpps
Size	632 inch ³	632 inch ³	86 inch ³
Delay	84us	2us	2us
Power	75W	91W	21W

viding times of hardware resources. To further compare the performance of OFS and different platforms, we have carried out several experiments among CPqD soft OFS, NetFPGA based OFS and ONetSwitch based OFS. The results are listed in table 2. ONetSwitch has the largest hardware flow table. And both soft OFS and ONetSwitch have soft flow tables to keep almost all the entries from the controller, so the probabilities to query controller is much lower than NetFPGA solution. We use Smartbits to generate traffic to test the performances. When we use packets with a size of 1500 Bytes (throughput1 in the table), both of the two hardware based OFS achieve wire speed of almost 1000 Mbps, but the forwarding speed of soft OFS is variable when CPU and flow table structures change. We try the most simple forwarding rules on our software based switch on a Core Duo 2.4GHz CPU machine, and it only achieved about 211Mbps. In the worst case with 64 Bytes packets (throughput2 in table), soft OFS can forward no more than 12.8K packets per second (pps), and the hardware assistant OFS can reach 1.5 Mpps. Since ONetSwitch has integrated PS inside Zynq, no extra host server is required like NetFPGA and the volume is much smaller. The OFS on ONetSwitch also show advantages in delay and power. Although ONetSwitch has many advantages, it also shows some limitations compared with the platforms with hosts. The ARM processor provides much less computing power than x86 based servers, so ONetSwitch does not fit for such kind of works that require more programming system resources.

4 Summary

The design of ONetSwitch presented in this paper is verified and commercially available to the community from Xilinx and its alliance partner company MeshSr. Another low end model of the ONetSwitch building with Zynq 7020 will also be ready for use with less cost in 2014 Q1/Q2. The picture of ONetSwitch with Zynq 7045 is shown in Fig. 3. Advantages compared with the designs on NetFPGA are: 1) ONetSwitch employs much more hardware resources, and therefore achieves more complex design and better performance. 2) No extra host server is required and the size is minimized. 3) Various interfaces are provided, which gives the researchers more flexibility. 4) Power monitoring circuit in ONetSwitch offer a chance for the research on green networking. 5) The design framework of the OFS provides a reference for the researcher to modify the data path of SDN. Detailed design and experiments of OFS on ONetSwitch will be discussed in future work.

References

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