# Extraction of Secrets from 40nm CMOS Gate Dielectric Breakdown Antifuses

by FIB Passive Voltage Contrast

Andrew D. Zonenberg

@azonenberg@ioc.exchange

Antony Moor, Daniel Slone, Lain Agan, Mario Cop

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# IOActive Presentation Content

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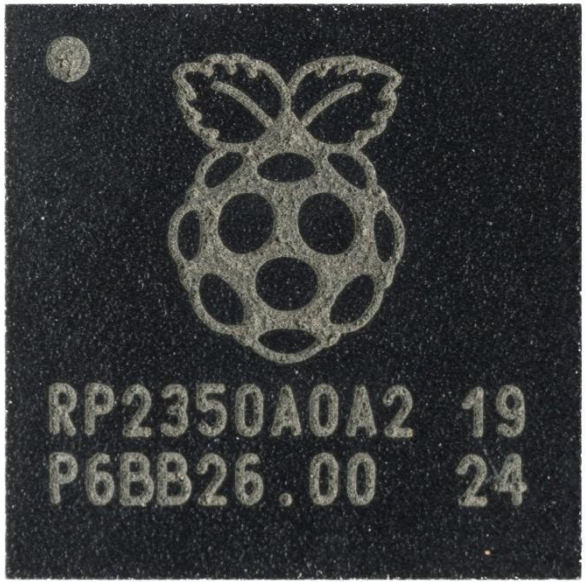
# So… what's the RP2350?

- Dual core MCU
  - Switchable M33 or RV32!
- 32 kB boot ROM
- 520 kB SRAM
- 8 kB ECC OTP (or 12 kB non-ECC)
- No internal flash
  - Boots from external QSPI flash
  - Supports signed images or nonsecure XIP





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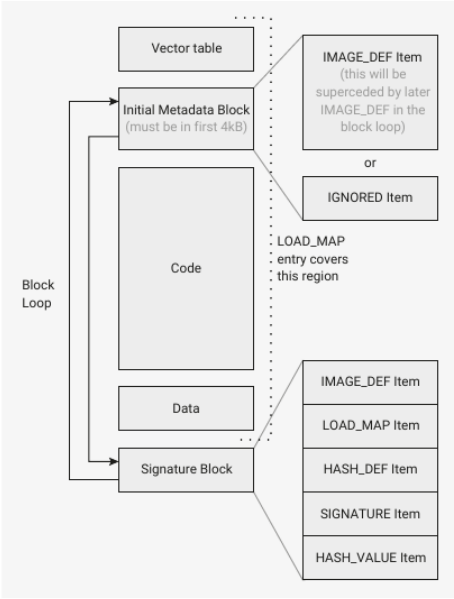
# Secure boot flow

- TL;dr: copy image from QSPI to SRAM
- Check signature
  - Pubkey + sig in image header
  - Hash of key burned into fuses
- If sig valid, run it
- Image is cleartext
  - Encrypted boot not *directly* supported





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# Encrypted boot flow

- Secure-boot a trusted, open source “stub”
- Stub copies main firmware blob to SRAM
- Can then decrypt using a key stored in fuses
  - Fuses support read protection so can’t dump via JTAG etc
  - Attacker who can read fuses could thus decrypt FW

# Let's do some OSINT

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Home / Synopsys IP / Foundation IP / NVM / Antifuse-Based Split-Channel 1T-Fuse Bit Cell for OTP NVM I

## Antifuse-Based Split-Channel 1T-Fuse Bit Cell for OTP NVM

At the heart of all Synopsys One-Time Programmable (OTP) Non-Volatile Memory (NVM) IP is the memory array, using a patented, area-efficient, antifuse bit cell – 1T-Fuse – that employs gate-oxide breakdown as a robust, non-reversible programming mechanism. This is a proven, reliable and secure technology that has been widely adopted and used in a broad range of applications and markets.

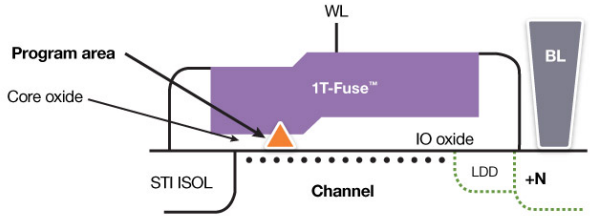


Figure 1: 1T-Fuse Bit Cell in Synopsys OTP NVM IP

The single-transistor OTP bit-cell (1T-Fuse) uses a unique split-channel architecture, where a single transistor gate covers both I/O (thick) and core (thin) oxides. The cell is programmed by a controlled, irreversible breakdown from the gate through the core (gate) oxide to the channel. The bit cell is programmed either with an embedded charge pump or through an external pin (at the tester, for example). The bit-cell is implemented using standard CMOS processes and requires no additional mask steps.

Gate oxide breakdown = antifuse

Cross section of memory bit cell

https://www.synopsys.com/dw/ipdir.php?ds=nvm_1t-bit-cell





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# Let's do some OSINT

Arrays are available from a few 100 bits to around 1M bit and may be cascaded for even larger macros. Synopsys memory arrays are very flexible and can replace multi-time programmable memory in many applications. Conversion to mask ROM is also simple.

Available in standard CMOS processes, Synopsys OTP memory arrays don't require additional mask layers or process steps and provide a viable alternative to mask ROM, eFuses and Flash memory. The reduced size of the single-transistor bit cell results in better yield, higher security, improved reliability and lower overall cost.

**Security Features**

The inherent security features of the 1T-Fuse bit-cell include:

- Programming is by permanent structural change in few atomic layers (located far from diffusion)
- No physical attack can reveal programmed state in FinFET or HKMG technologies
- No leakage in non-programmed state
- State cannot be changed through exposure to high temperature, voltage or radiation
- No charge or voltage involved in state retention (unlike floating gate NVM, e.g. flash)
- State of memory (even for a few bits) is virtually impossible to detect using physical attack or reverse engineering techniques

That sounds like a challenge…

https://www.synopsys.com/dw/ipdir.php?ds=nvm_1t-bit-cell





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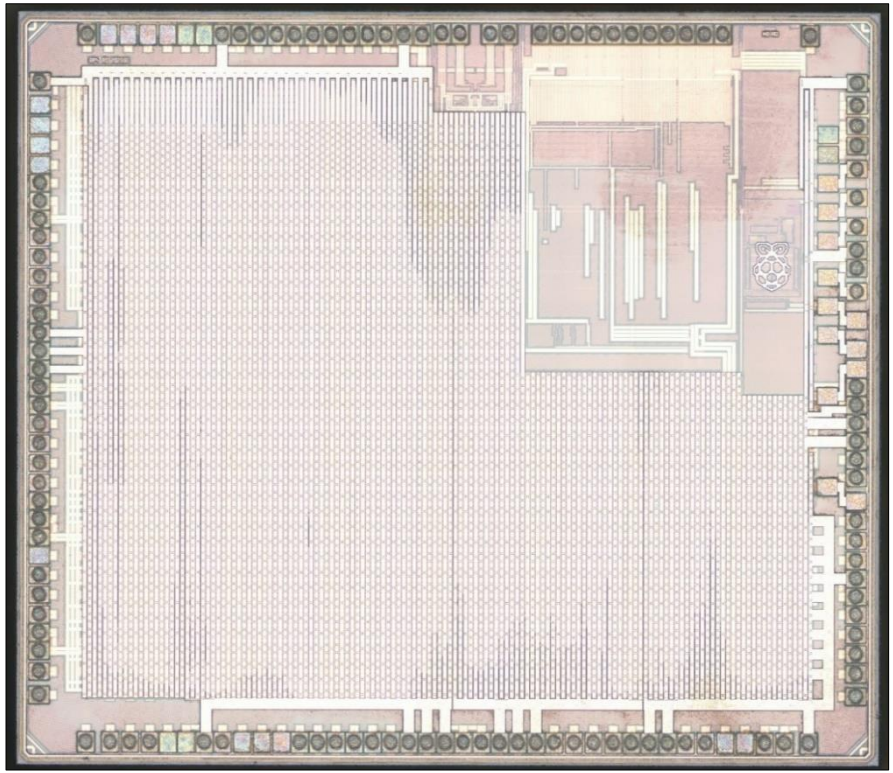
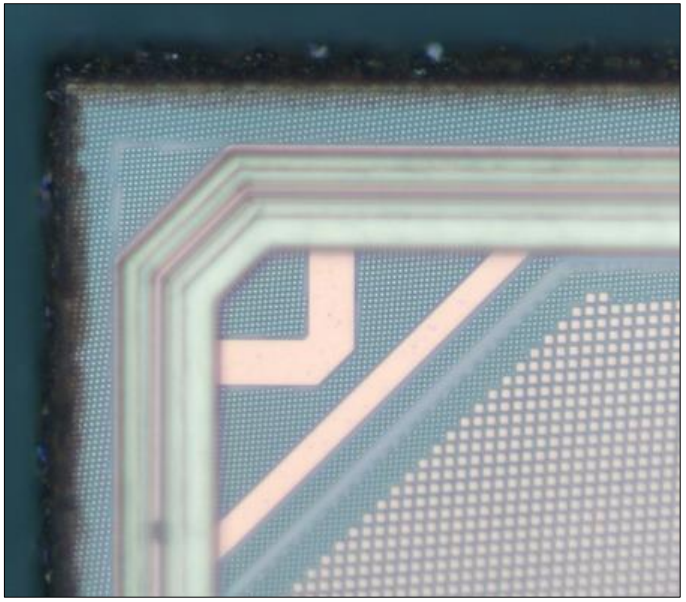
# How to get the key?

- Decap the chip
- Find the fuses
- Figure out a way to dump the bits
  - But it’s “virtually impossible”…

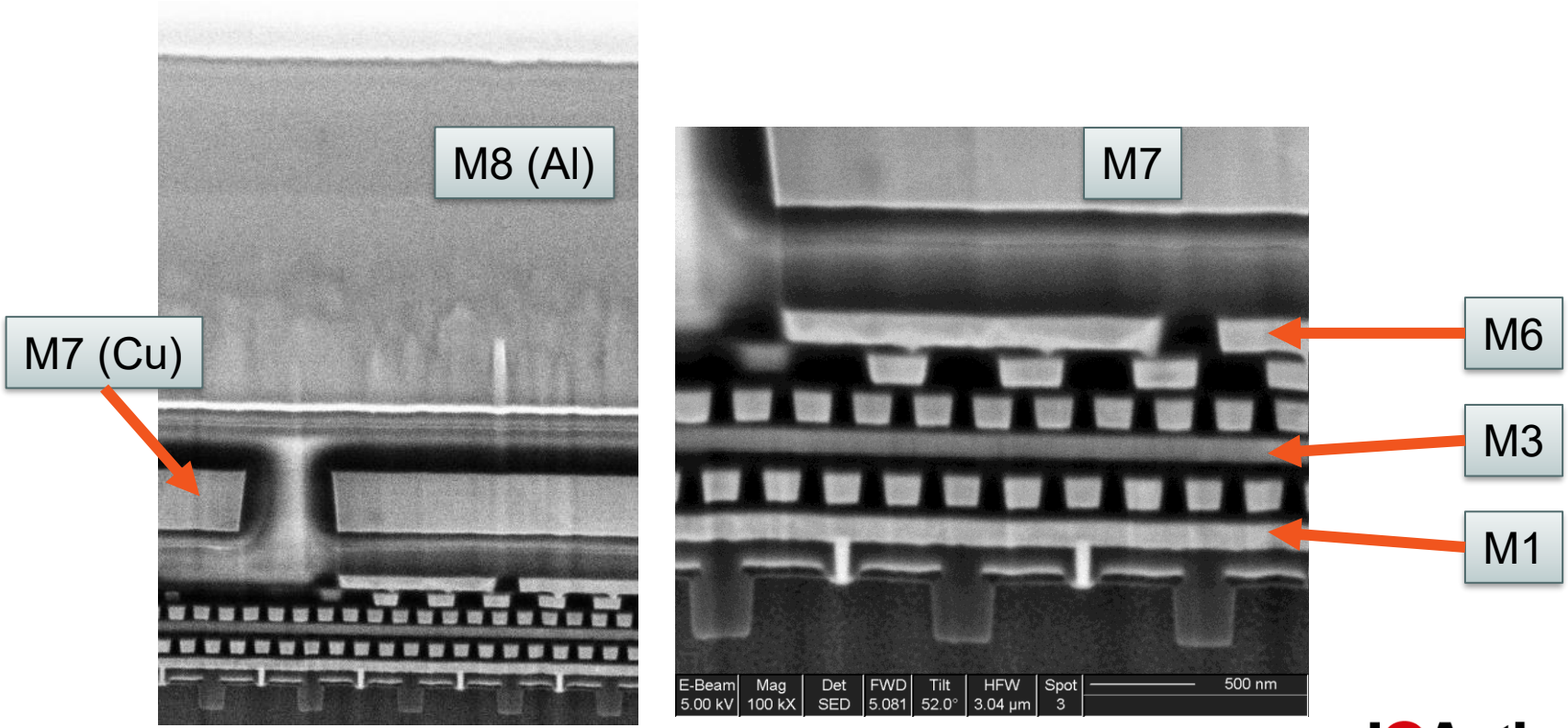
# Top metal (M8) overview





2.218 x 2.477 mm (5.493 $mm^2$)

# 40nm TSMC (7 Cu + 1 Al)





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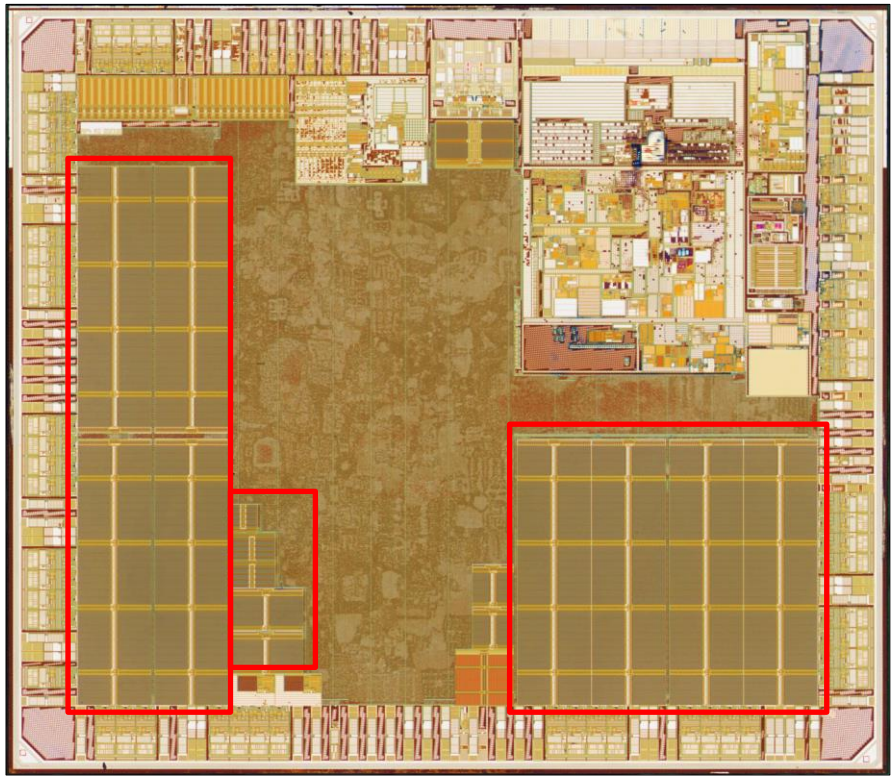
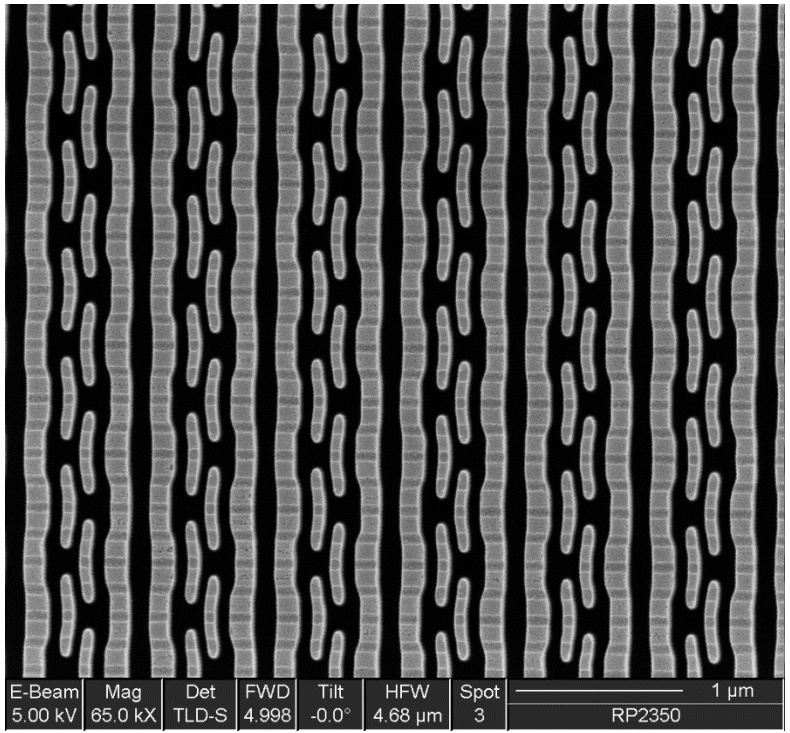
# 6T SRAM (single port)







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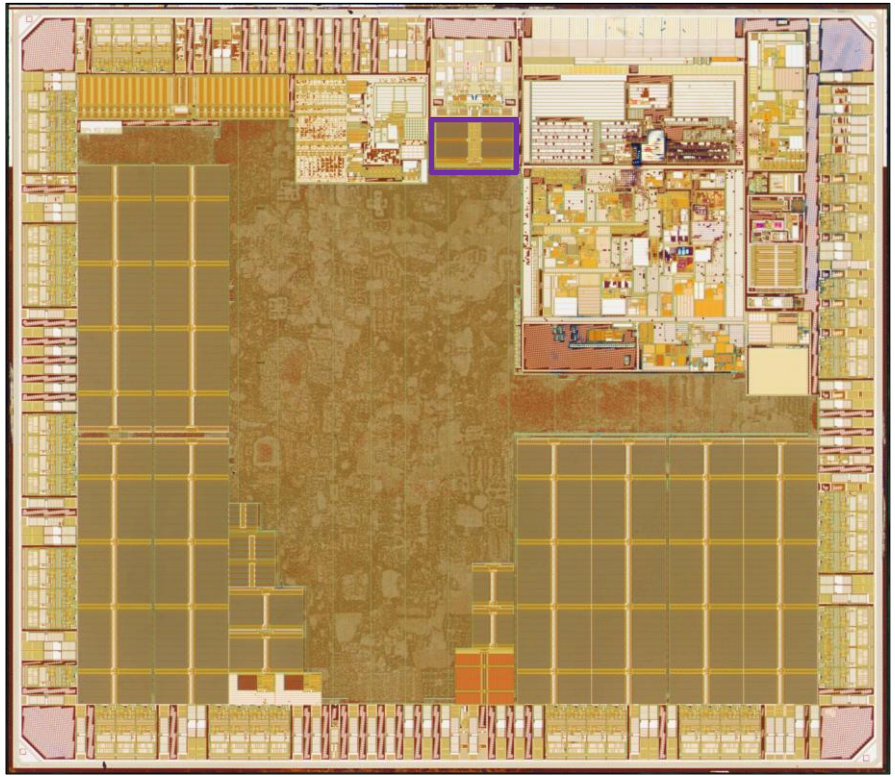
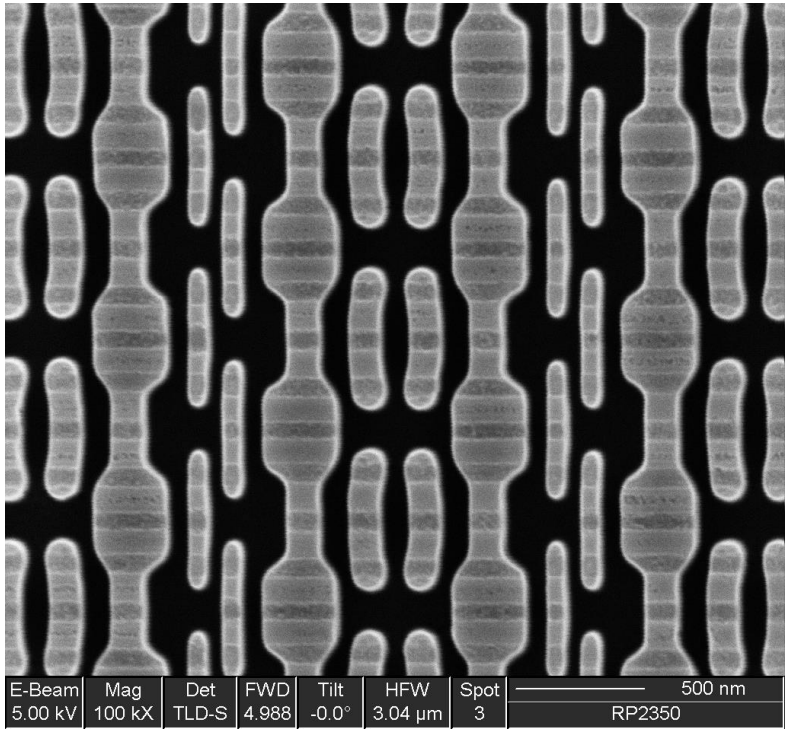
# 8T SRAM (dual port)







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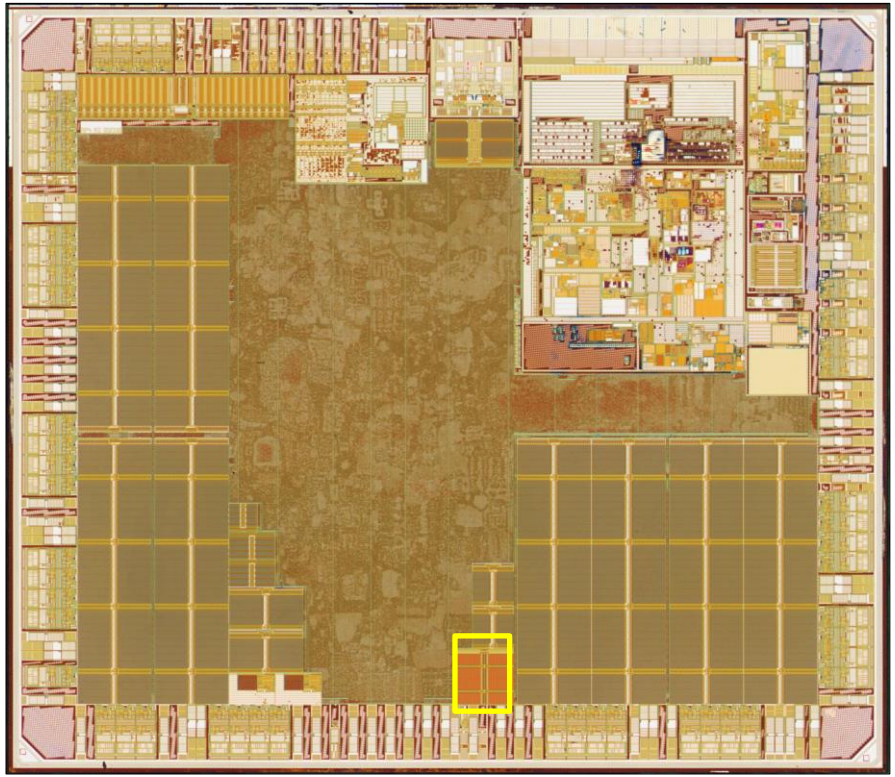
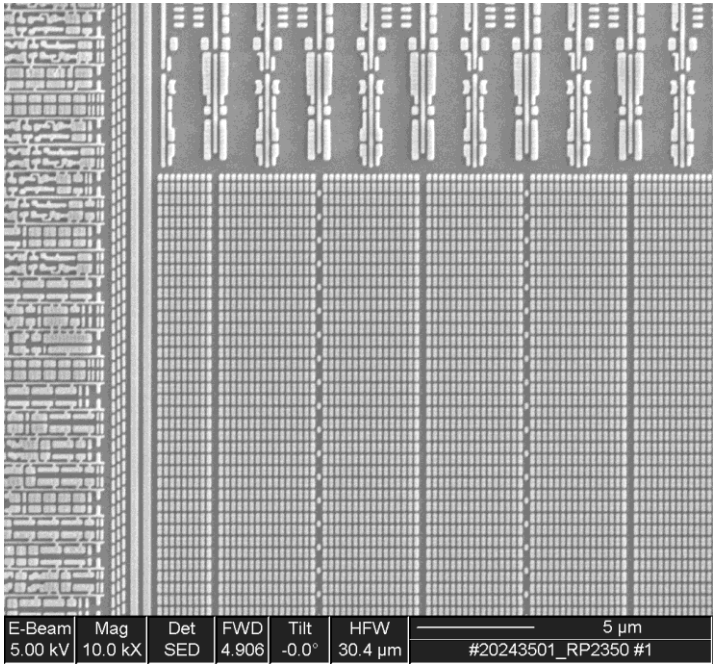
# Mask ROM (no bits visible, likely on M1)






Boot ROM is open source

No point spending time dumping it





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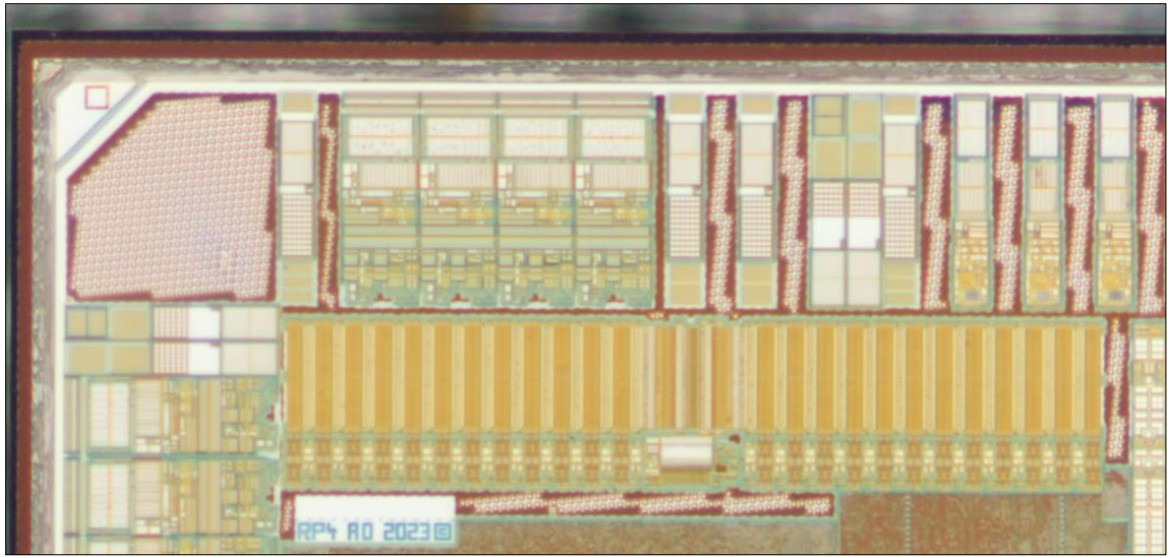
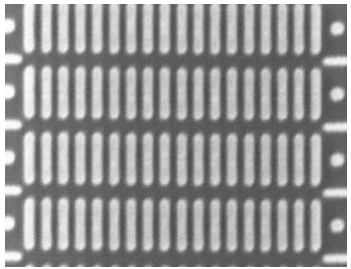
# 0w0 what's this?




- Not SRAM
- Not ROM
- Not flash
- Looks to be 24 cols
- Fuses are 24 bits
- Hmmm…







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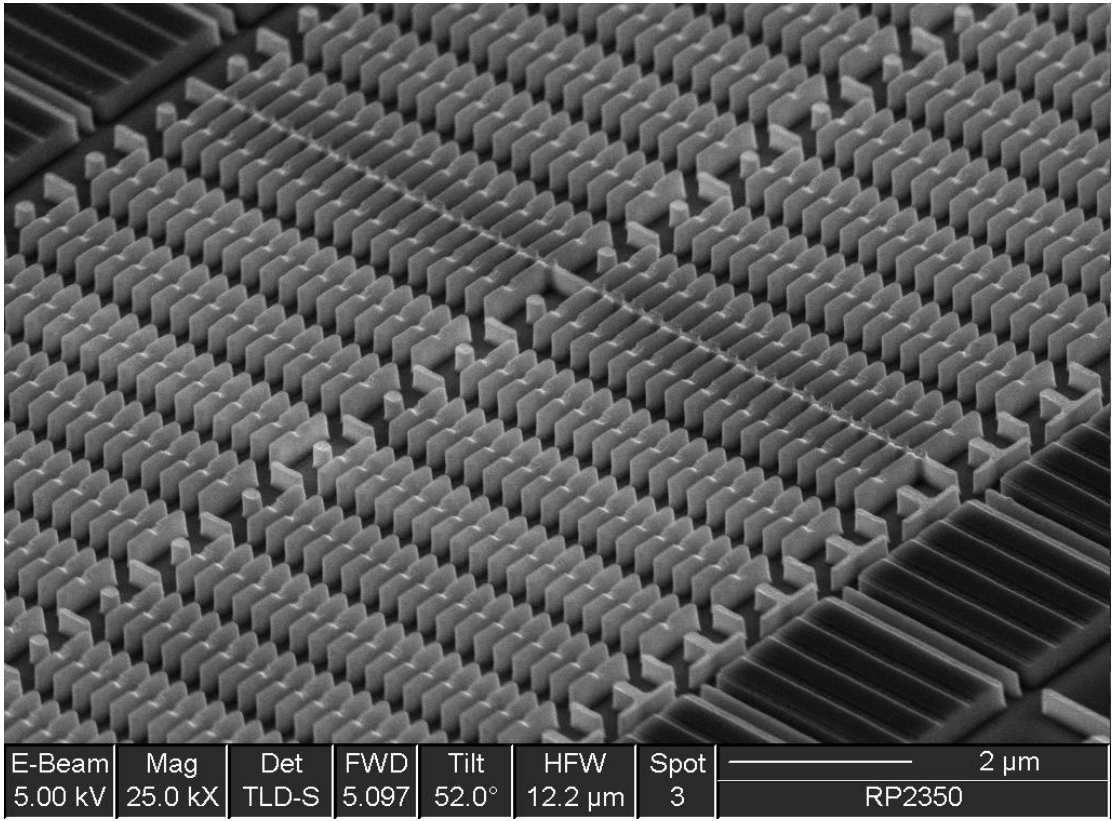
# Closer…





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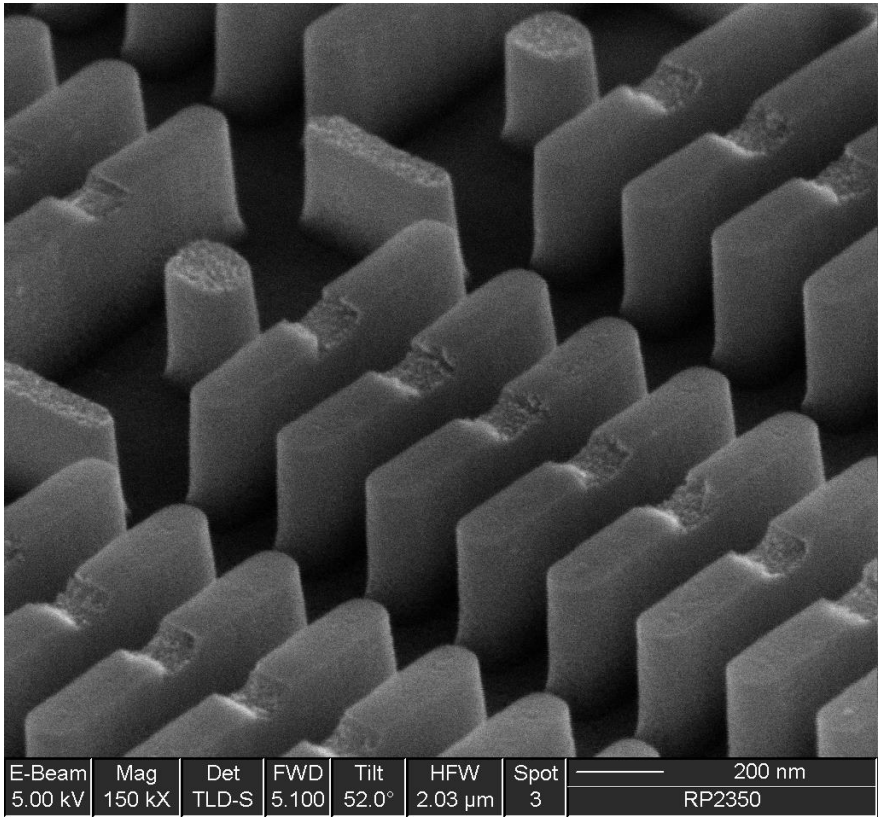
# Closer!





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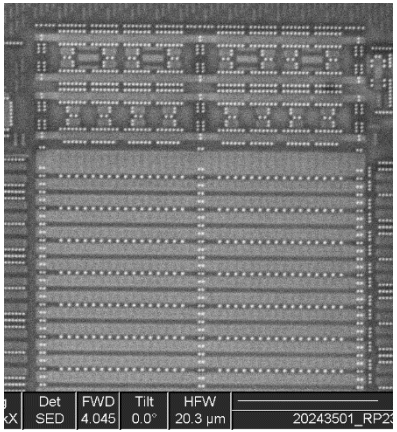
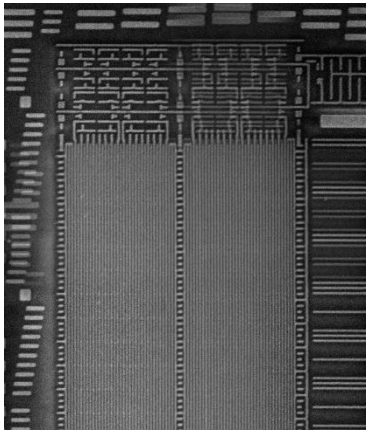
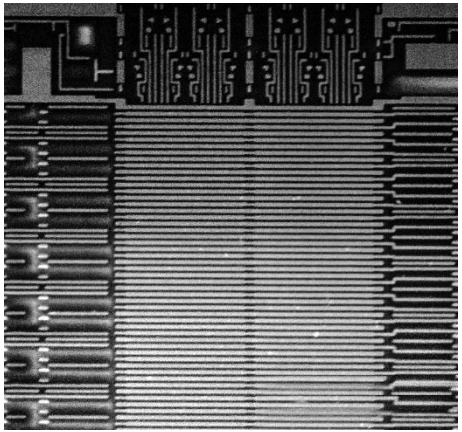
# Multi layer overview



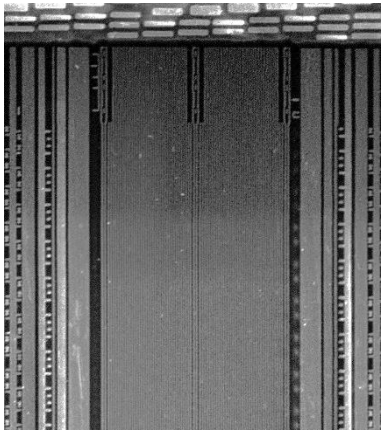

Poly
Contact



M1



M2



M3





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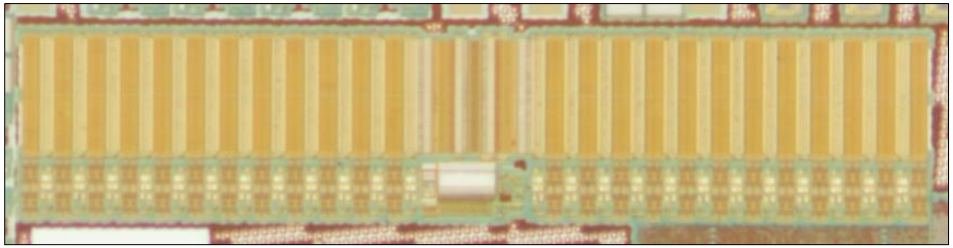
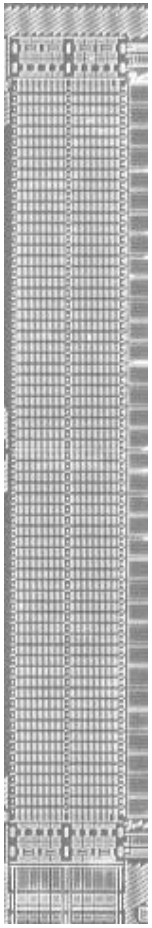
# High level address map

- 24 columns: matches the 24-bit fuse width
  - Each column is probably all rows of one bit
  - Don’t know which column is which bit plane yet
- 2 x 2 sub-arrays in each bit plane
  - 4096 words in the whole memory
  - Each sub-array must be 1024 words









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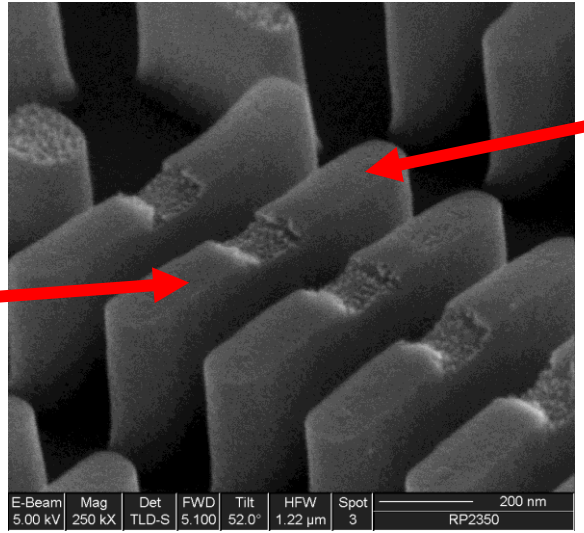
# Subtract the dummy features and…

- 16 columns x 32 rows per sub array
- 512 tiles for 1024 bits
- Each tile must store two bits





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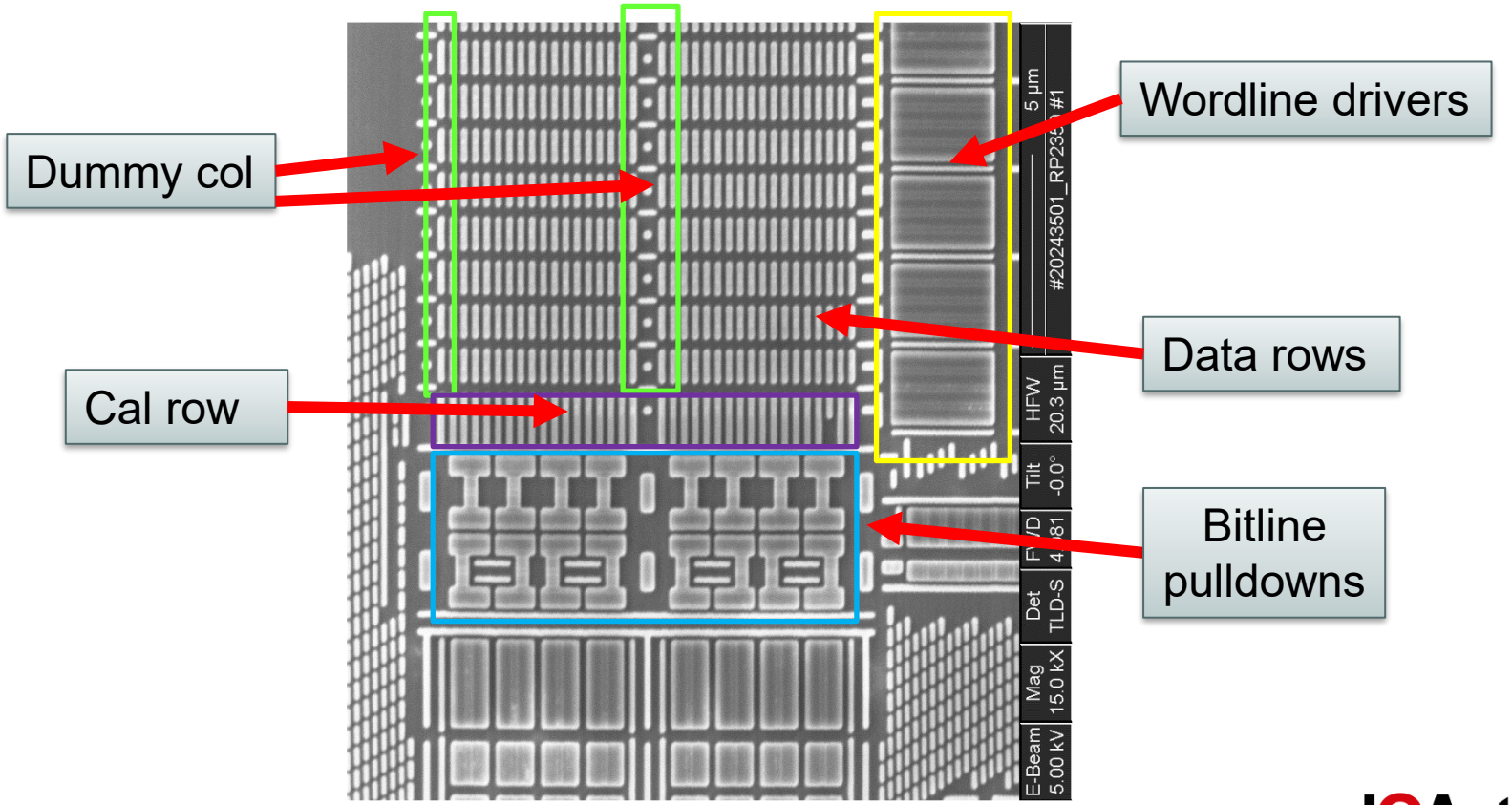
# Bottom of a single bit plane (substrate)





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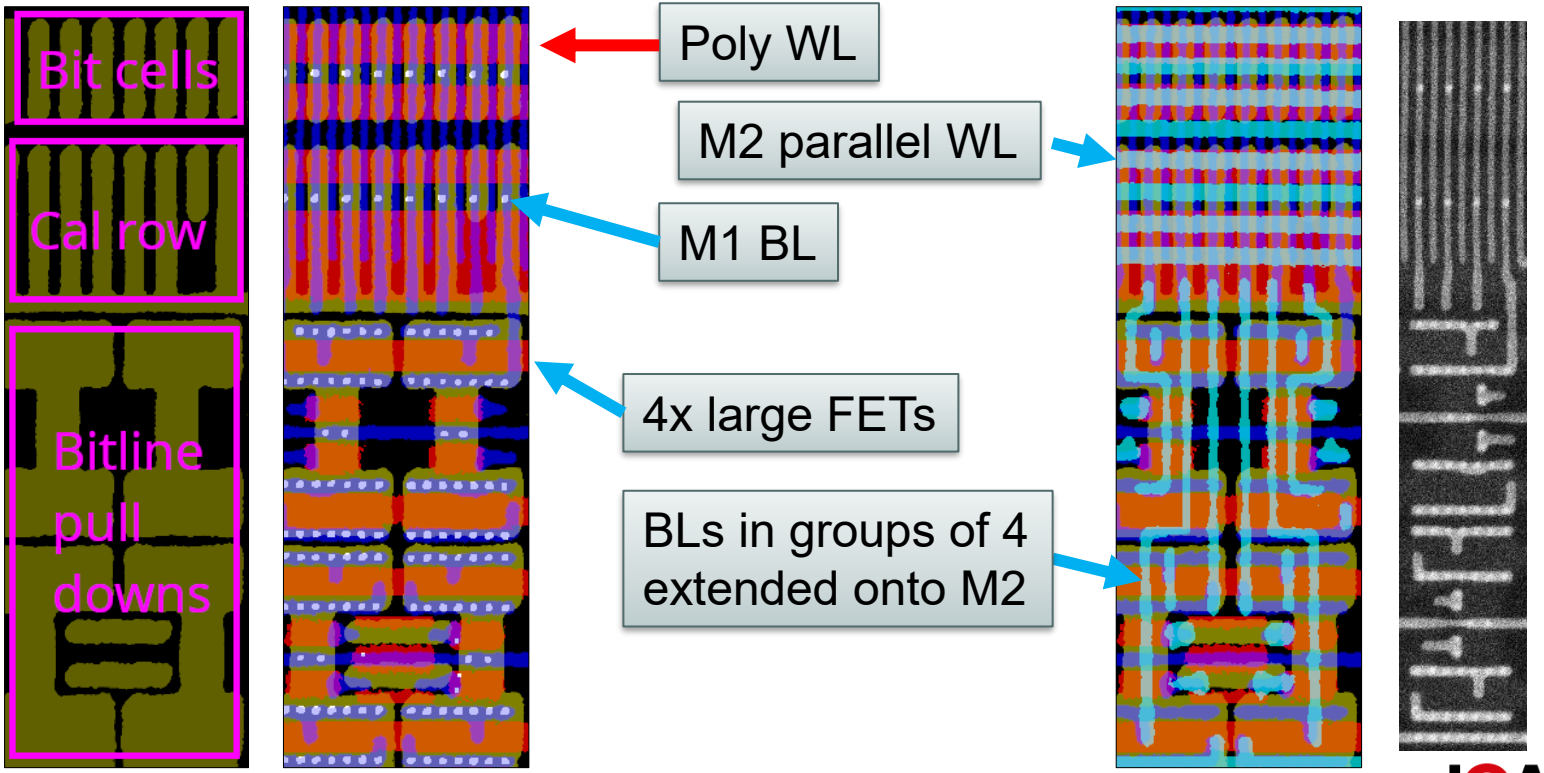
# Contacts, poly, M1, M2





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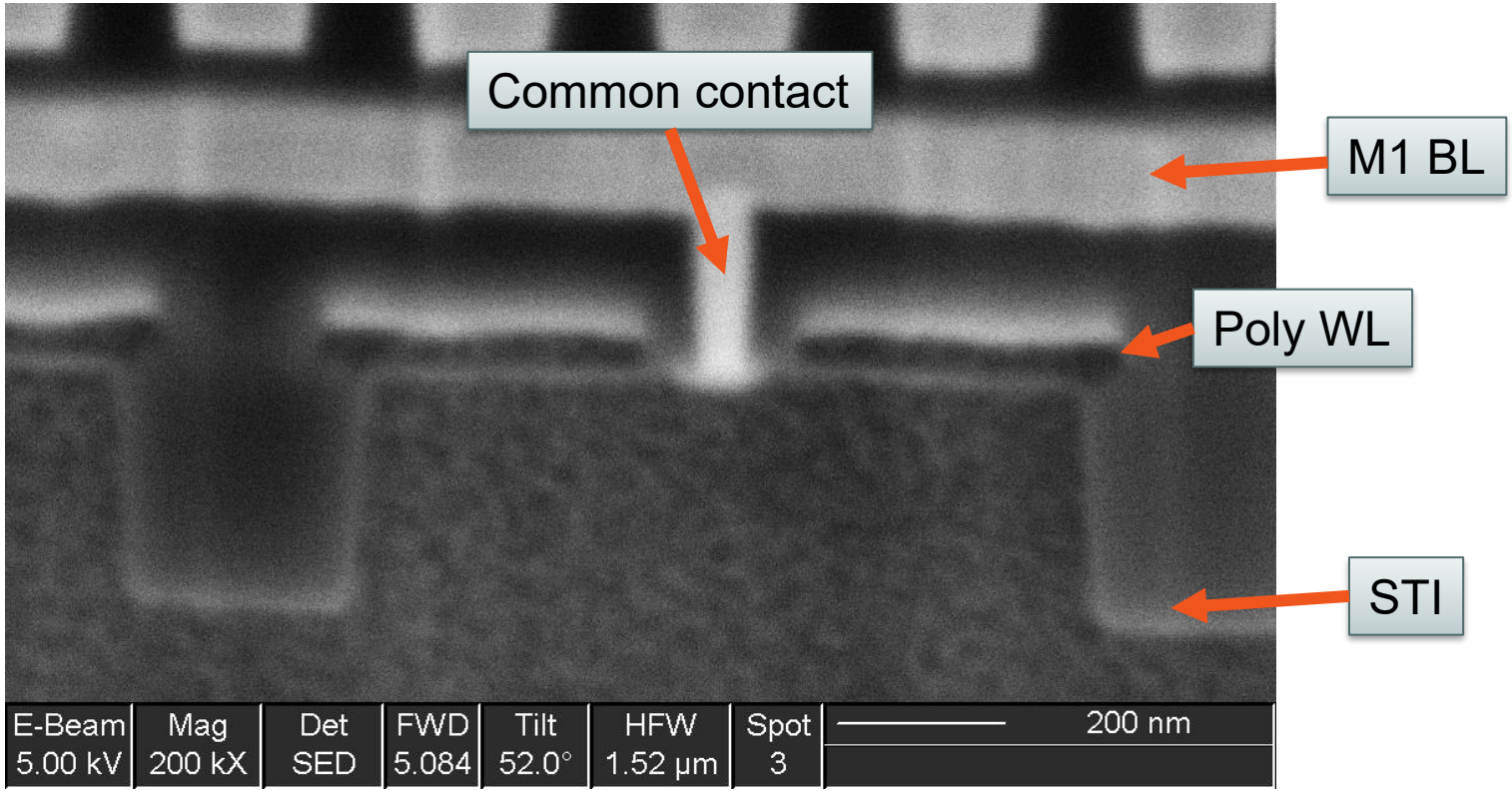
# Bitcell pair in cross section





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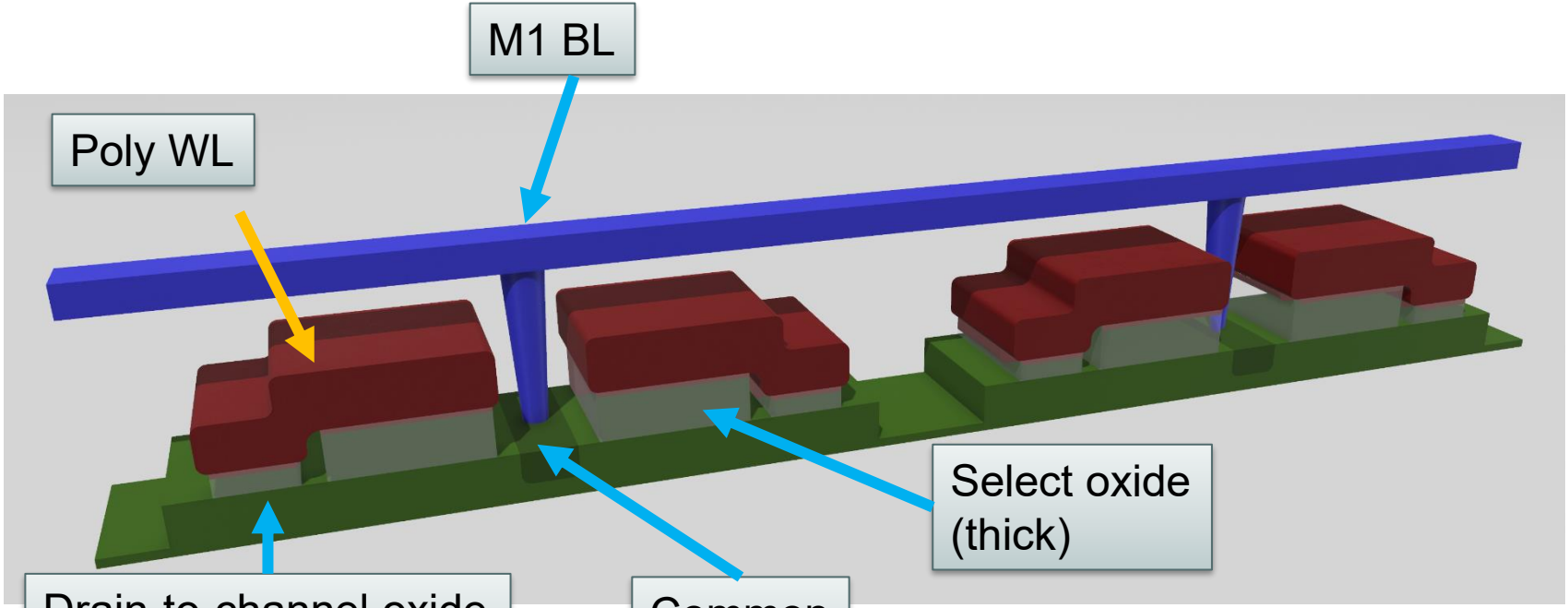
# Two rows of bit cells (not to scale)





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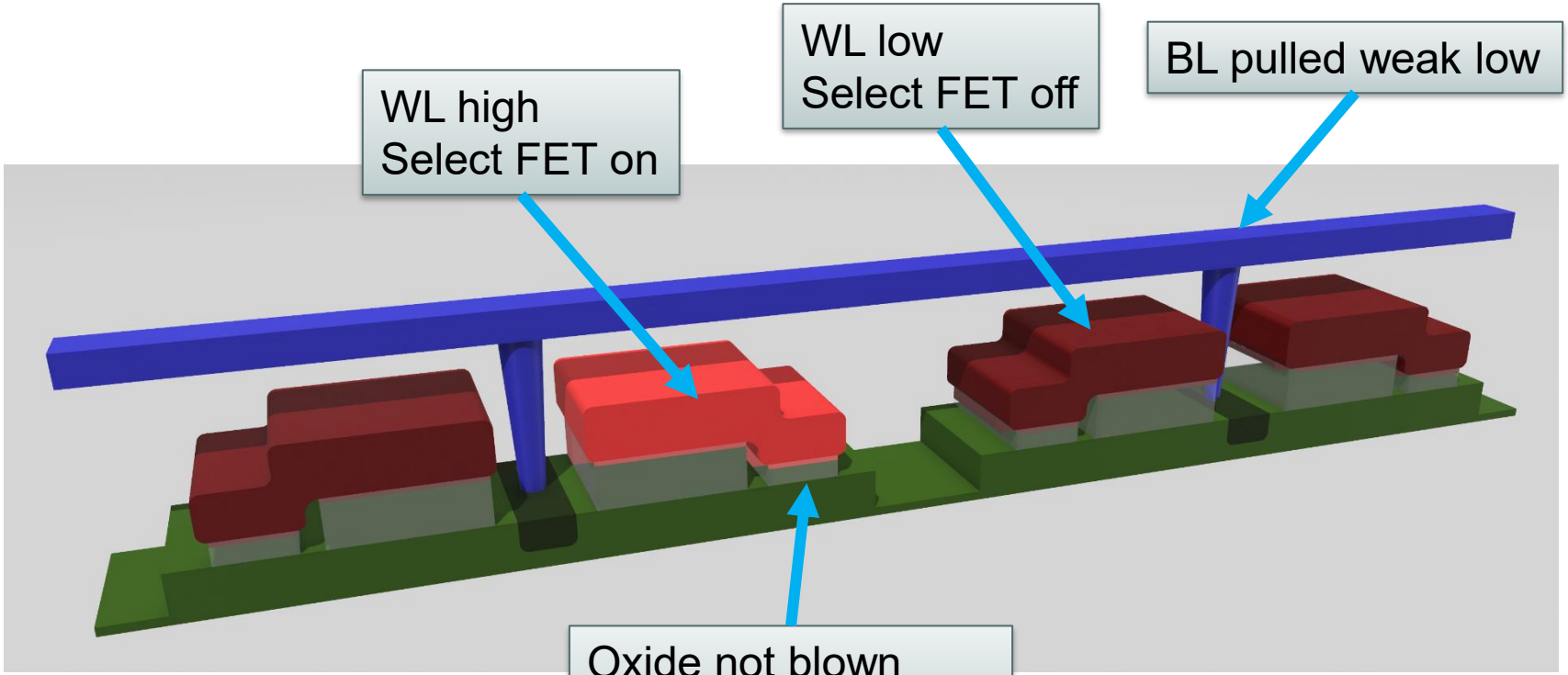
# Reading blank (0) bit





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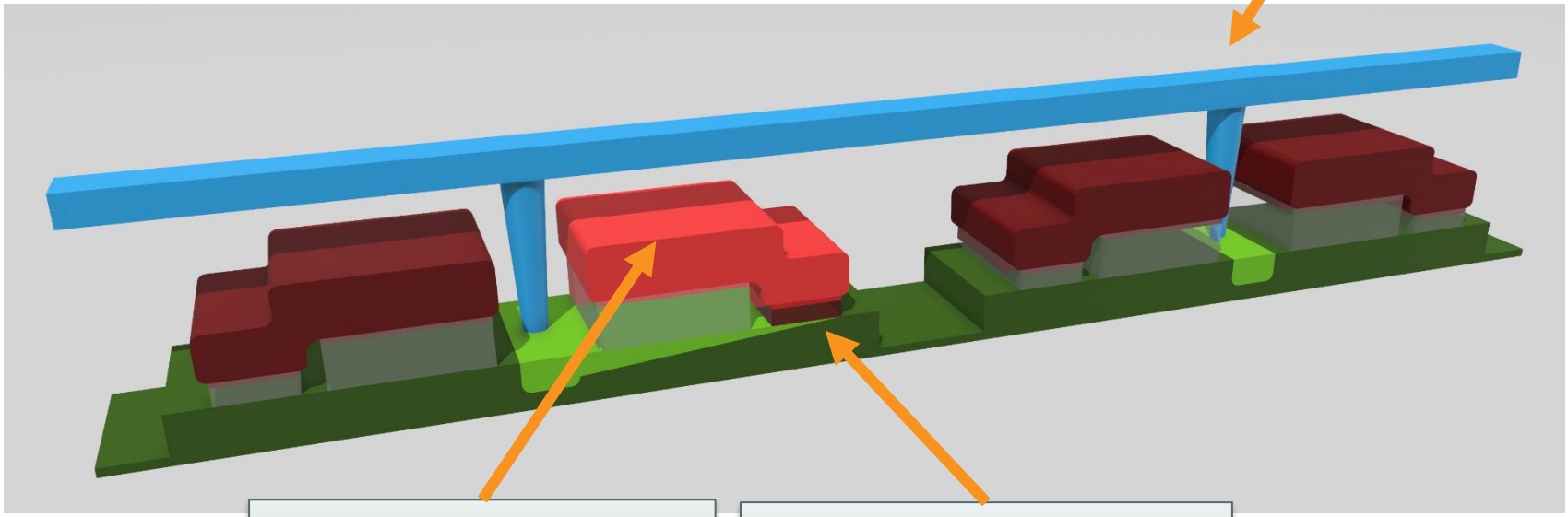
# Reading programmed (1) bit

BL driven high
Overrides pulldown



WL over channel high
Select FET on

Oxide blown
N+ poly *is* drain of FET





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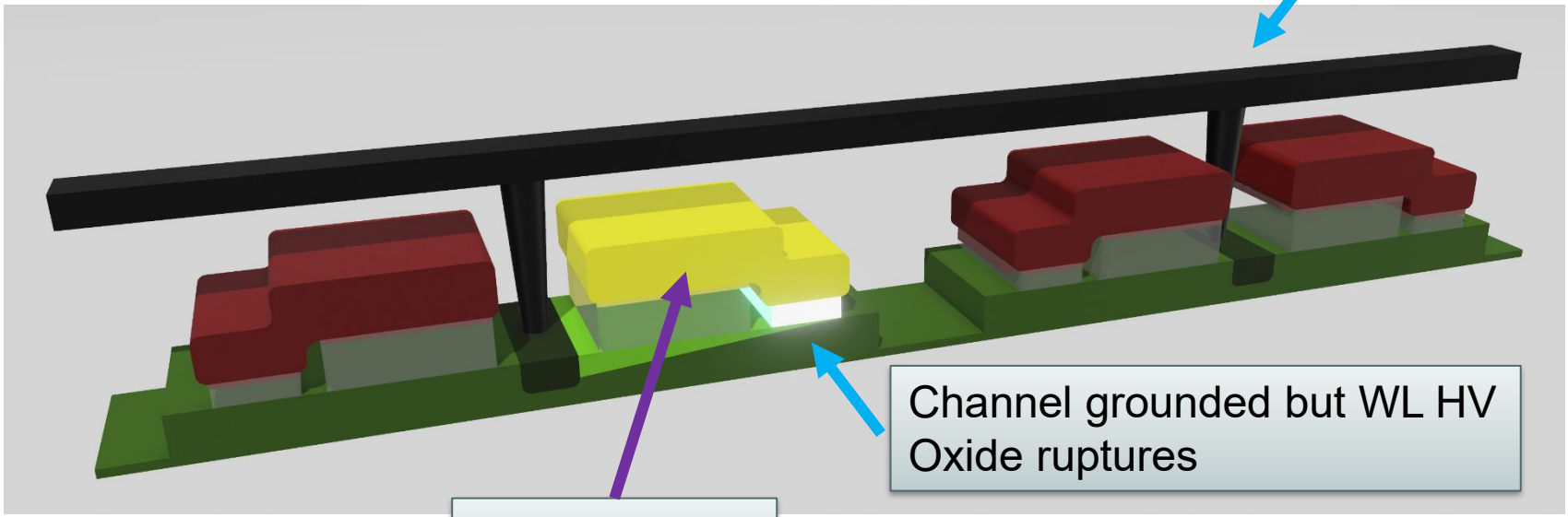
# Programming 0 bit to 1





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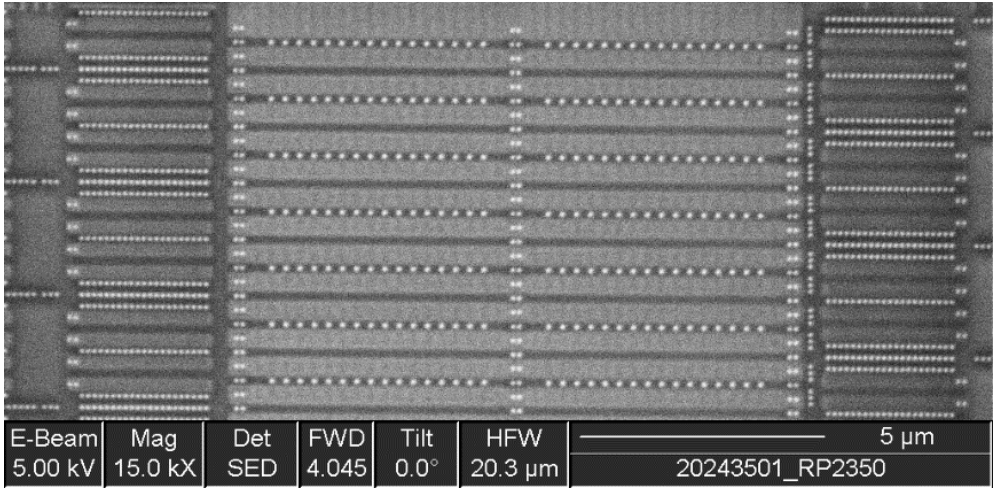
# What if we could just see the bits?

- But…
  - All bits look the same in SEM
- Maybe a different technique?





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# What if we could **see voltages**?

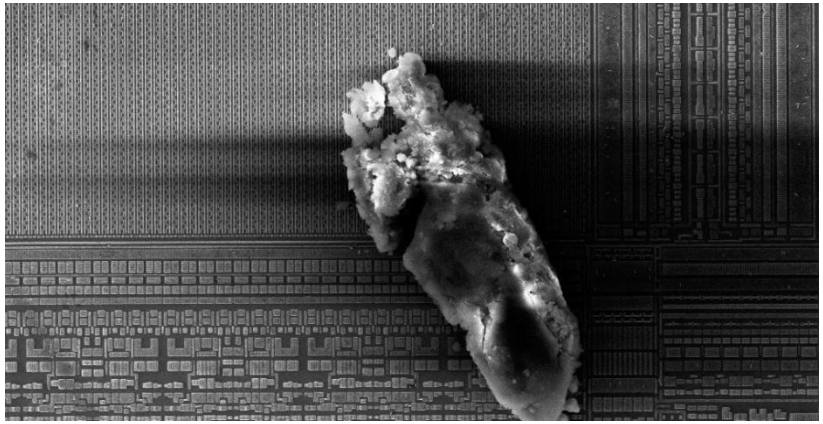
- Voltage contrast imaging!
  - Passive VC: beam used for imaging + biasing
  - Active VC: beam used for imaging, external bias

# Particle beam imaging recap

- Raster a beam of charged particles over the specimen
  - $e^-$ (SEM), $Ga^+$ (FIB) most common
- Beam interacts with sample atoms
- Detect these interactions somehow
  - X-rays
  - Secondary electrons
  - Backscattered electrons
  - Cathodoluminescence

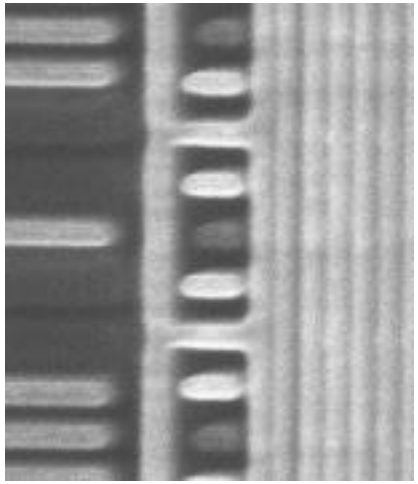
# Particle beam imaging w/ charged sample

- SEs are low energy / low mass – easily deflected
- Charged samples are normally bad for SE imaging
  - Causes image shifts, dark spots, difficulty imaging
  - This is why we coat
- But we can put this to use!



Positively charged dust speck
Attracts SEs from adjacent areas

# Voltage contrast imaging



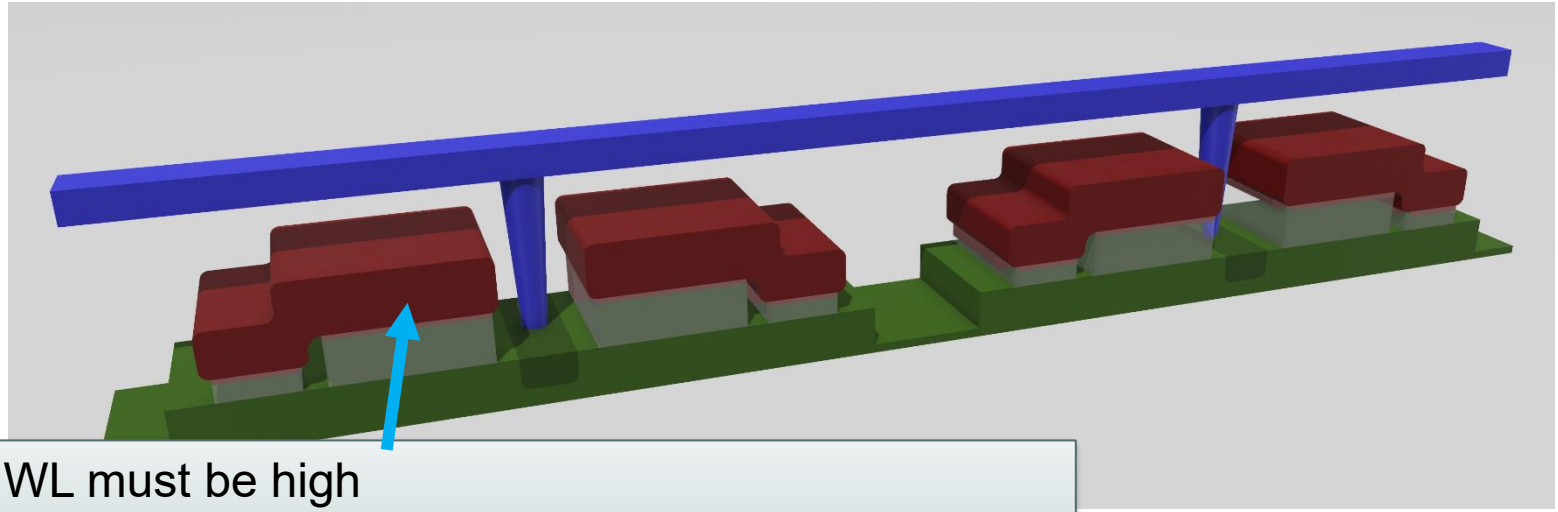
- **Deliberately** charge sample surface
- Charged polygons attract / repel SE's
  - Causes visible brightness shifts in the image
  - Positive charge: attract SE's, less detected, dark image
  - Negative charge: repel SE's, more detected, light image
- Infer memory state, connectivity, etc

# Passive voltage contrast (PVC)

- Imaging beam *also injects charge* into DUT
  - No probe or external power source needed
- Less precise control
  - Everything you can see is also having charge injected
  - Scan rate, coatings, accelerating voltage, etc. affect results
  - Balance charge deposition and bleed-off

# Can’t do SEM PVC on this bitcell structure

- Electron beam is negatively charged



WL must be high
If select FET is off, we see nothing
So injecting negative bias with e-beam is useless

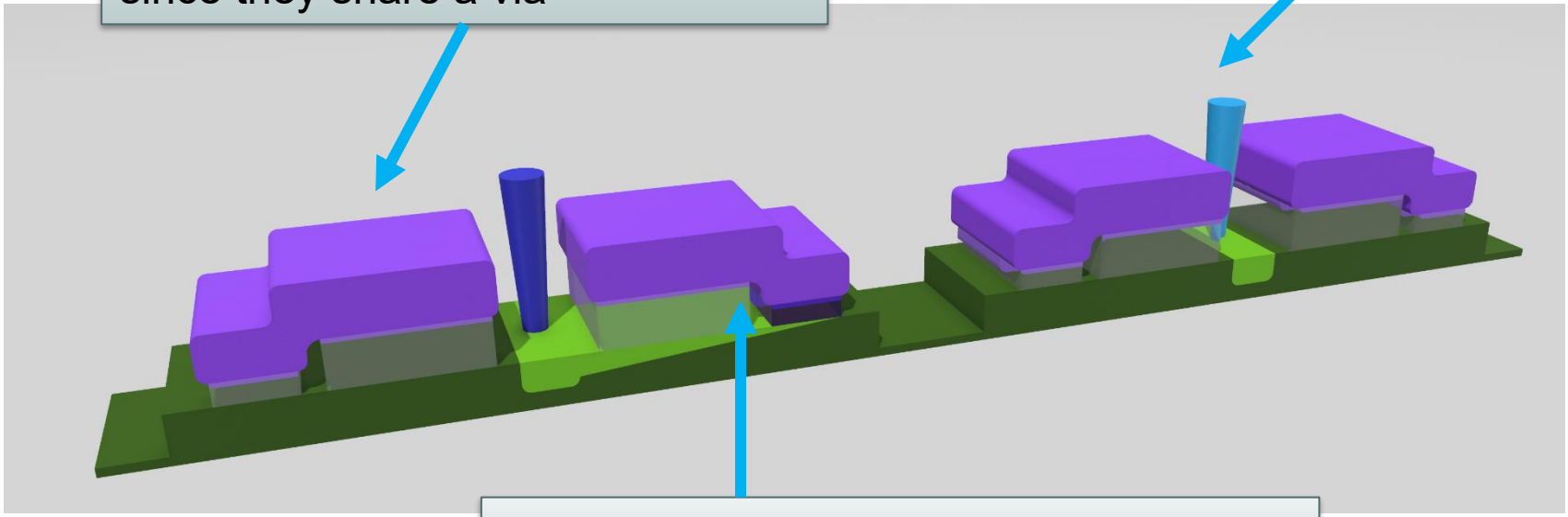
# FIB PVC

- Use positively charged $Ga^+$ beam
  - Injects positive charges into sample
- Destructive (sputters DUT surface)
  - Use low beam current, work fast to minimize damage

# Mass fuse readout via FIB PVC

Both halves on simultaneously
Cannot distinguish between halves since they share a via

Deprocess to contacts
No BL remaining



Ion beam injects positive charge on WLs
Positive $V_{gs}$ = bitcell transistor on





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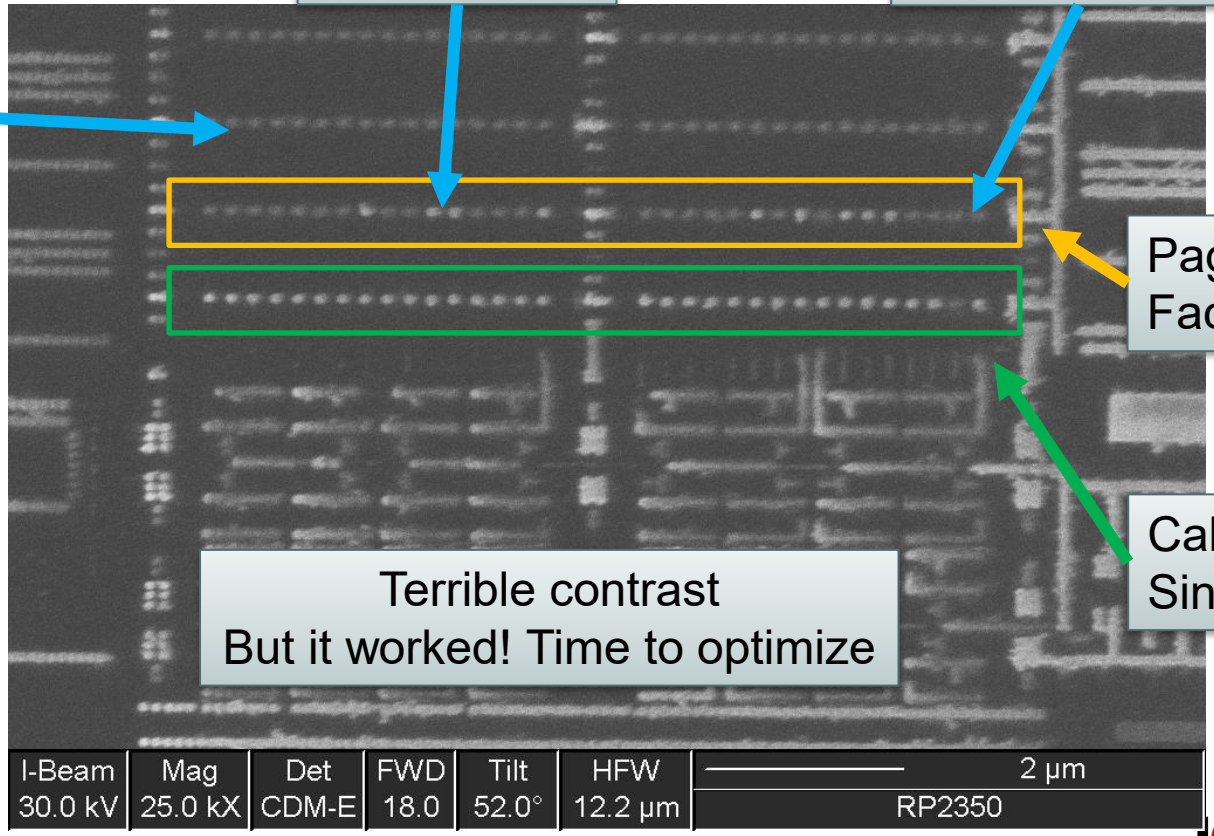
# First light





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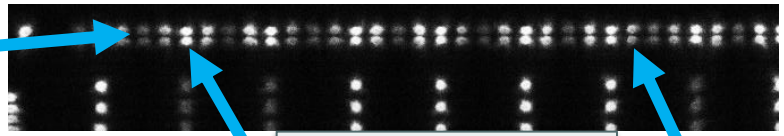
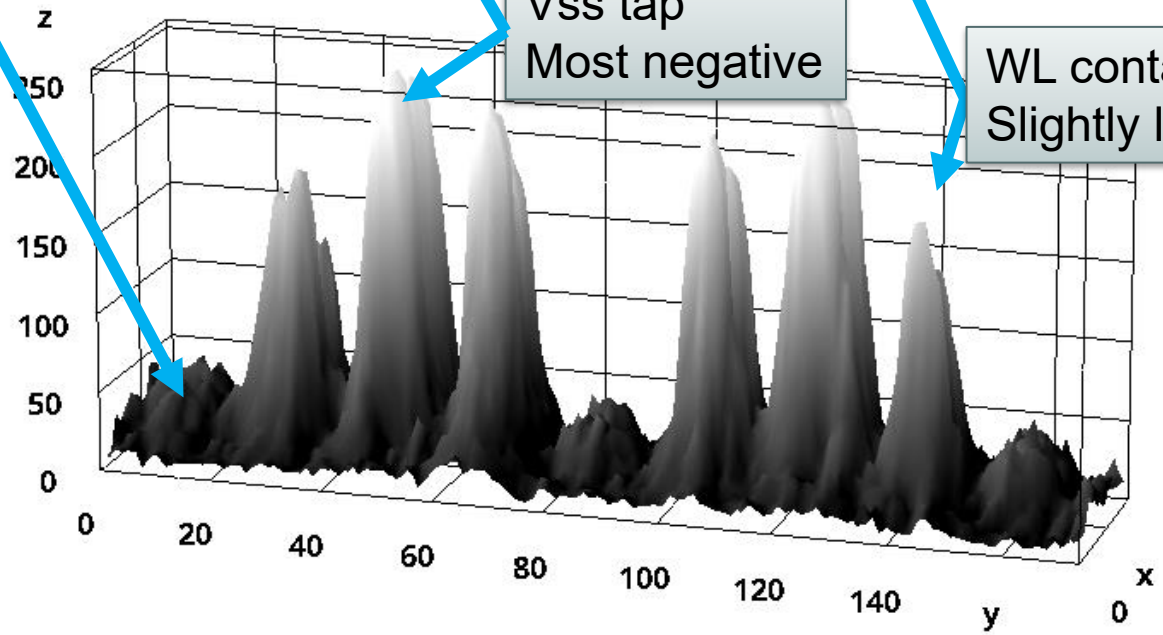
# Qualitative voltage measurements via PVC

Vdd tap
Least negative



Vss tap
Most negative

WL contact
Slightly less negative





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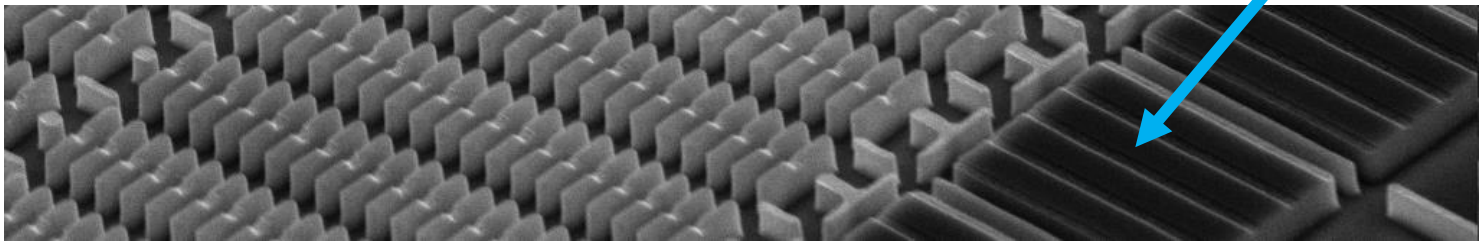
# Proposed Contrast Mechanism

- WL builds up *some* positive charge
- But most of it leaks to ground
- Likely sits at a few hundred mV
  - Around $V_t$, bitcell transistors starting to conduct
  - Can pass ~10 pA with reasonably low $V_{ds}$





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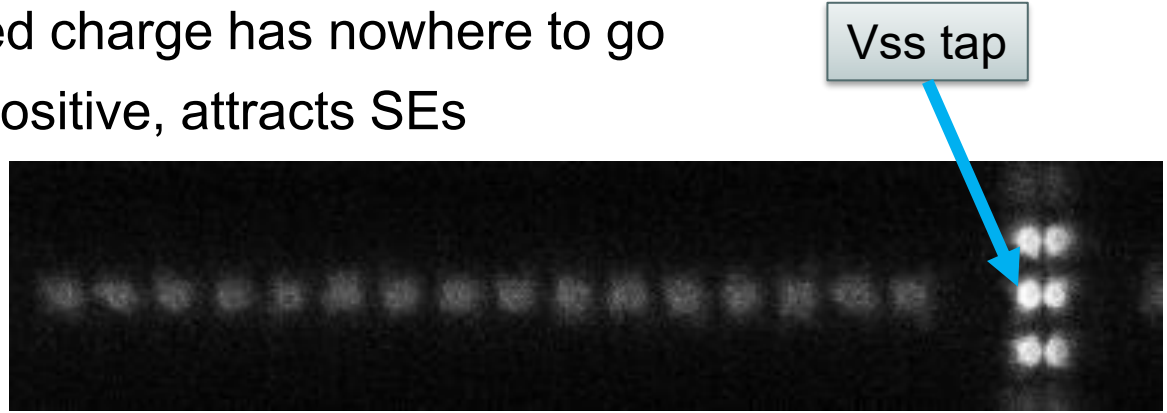
# Proposed Contrast Mechanism

- Unprogrammed bit
  - BL is floating even though select FET is on
  - Beam-induced charge has nowhere to go
  - BL strongly positive, attracts SEs
  - Dark image





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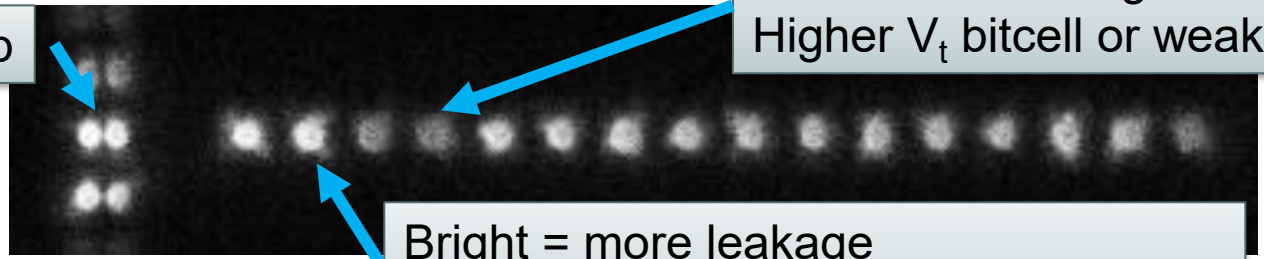
# Proposed Contrast Mechanism

- Programmed bit
  - BL is connected to WL by $R_{ds}$(on) of select FET
  - WL (thus BL) is at very low positive voltage
  - Light image, but a bit darker than grounded
  - Can see process variation!



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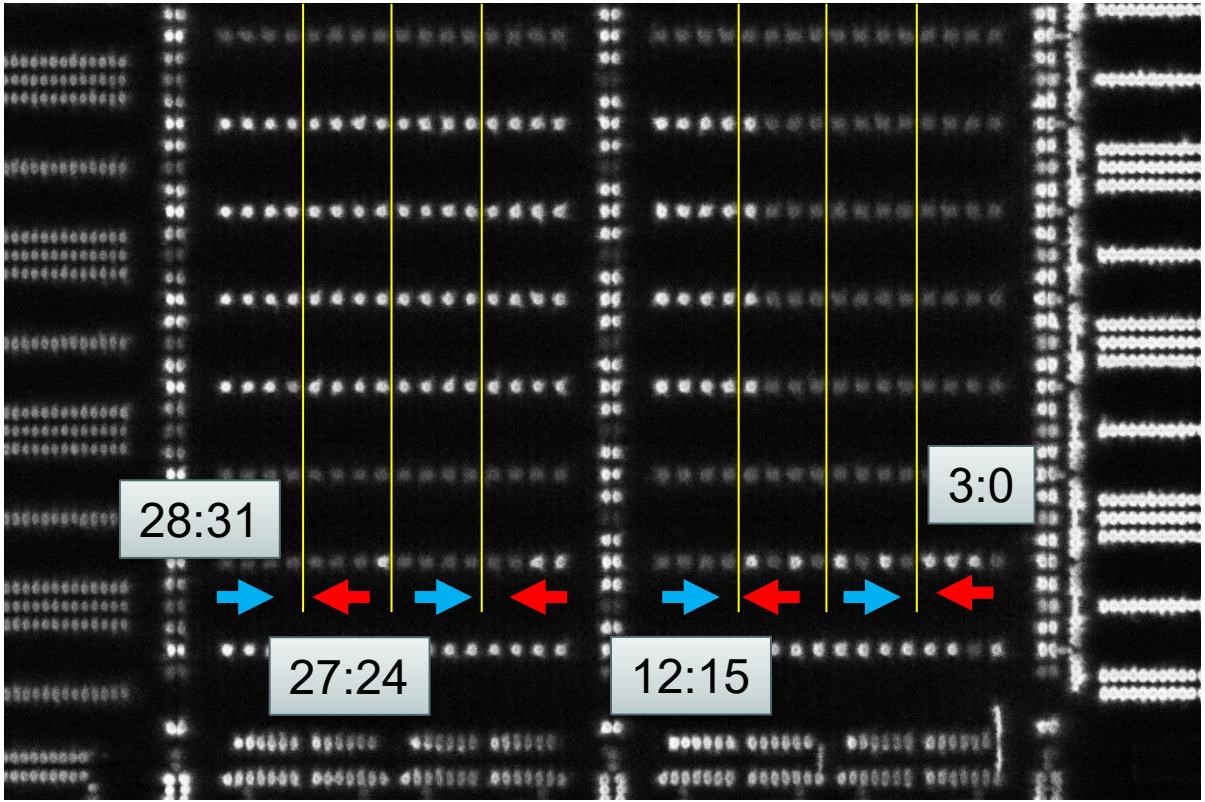
# Reversing the address map

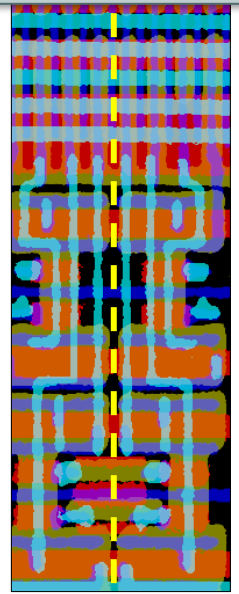
- Program our own test patterns
  - Different data in each bit plane to ID columns
  - Horizontally + vertically asymmetric to ID mirroring
  - Find the challenge key
  - And, of course, have some fun in the process

# Column ordering

West side of array shown
East side mirrored L-R




Even/odd nibbles mirrored







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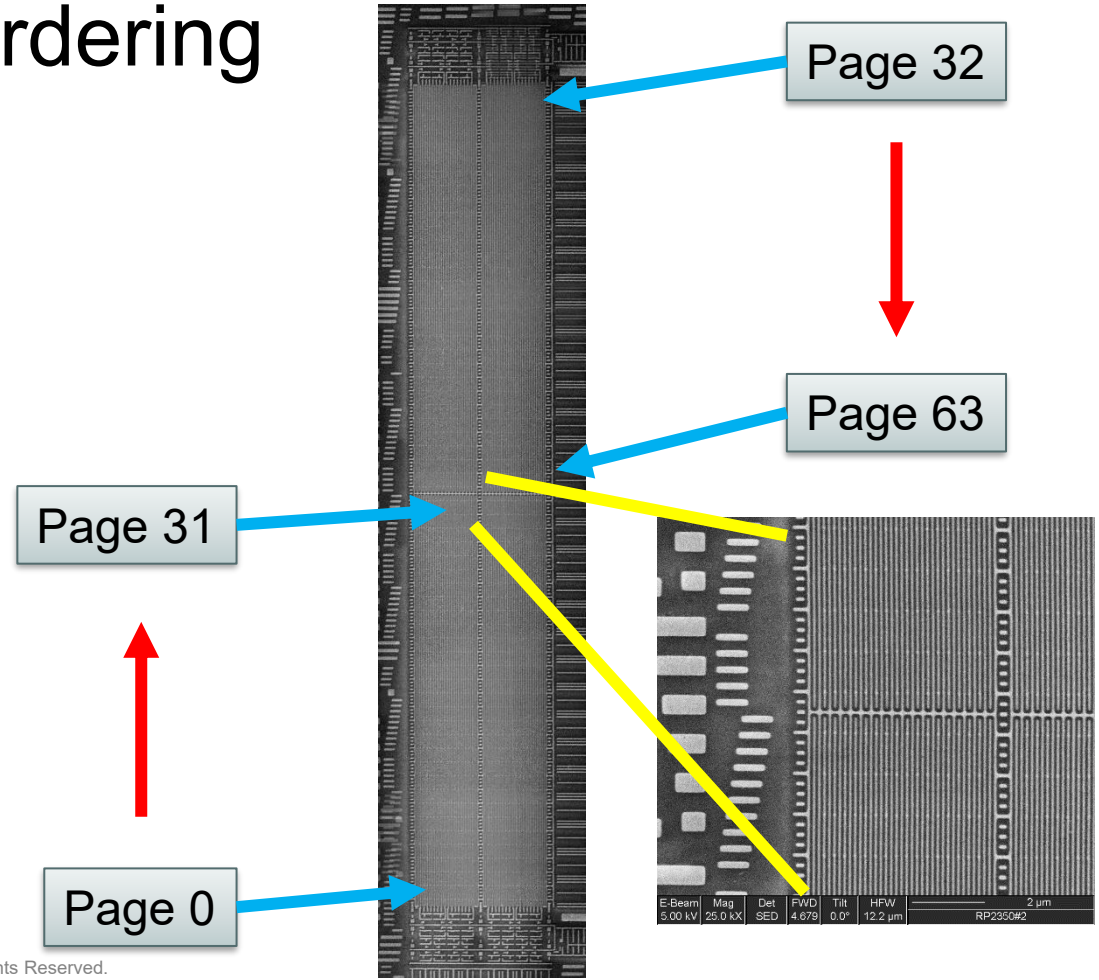
# Row ordering

M1 view

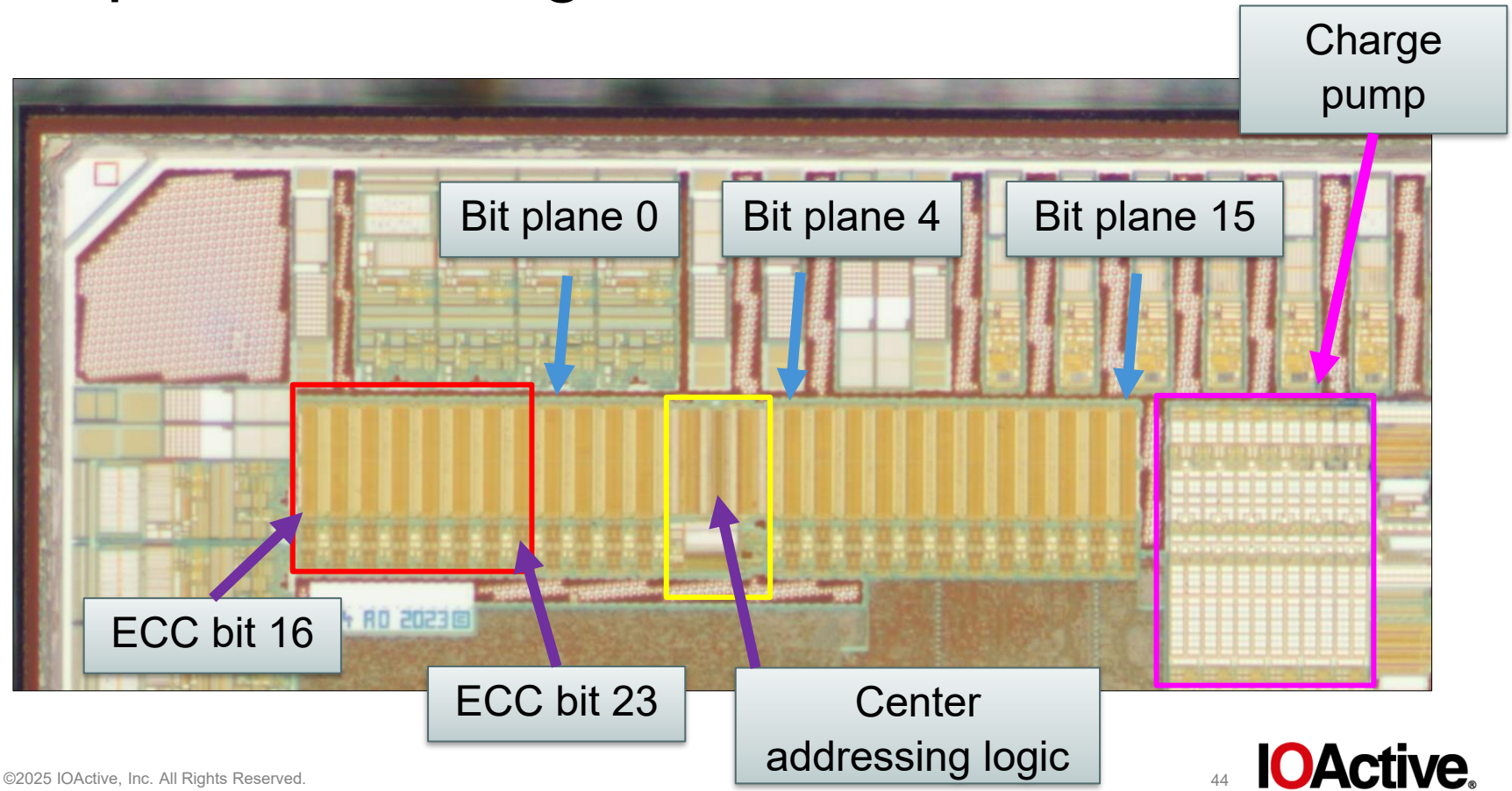







IOActive.

# Bit plane ordering

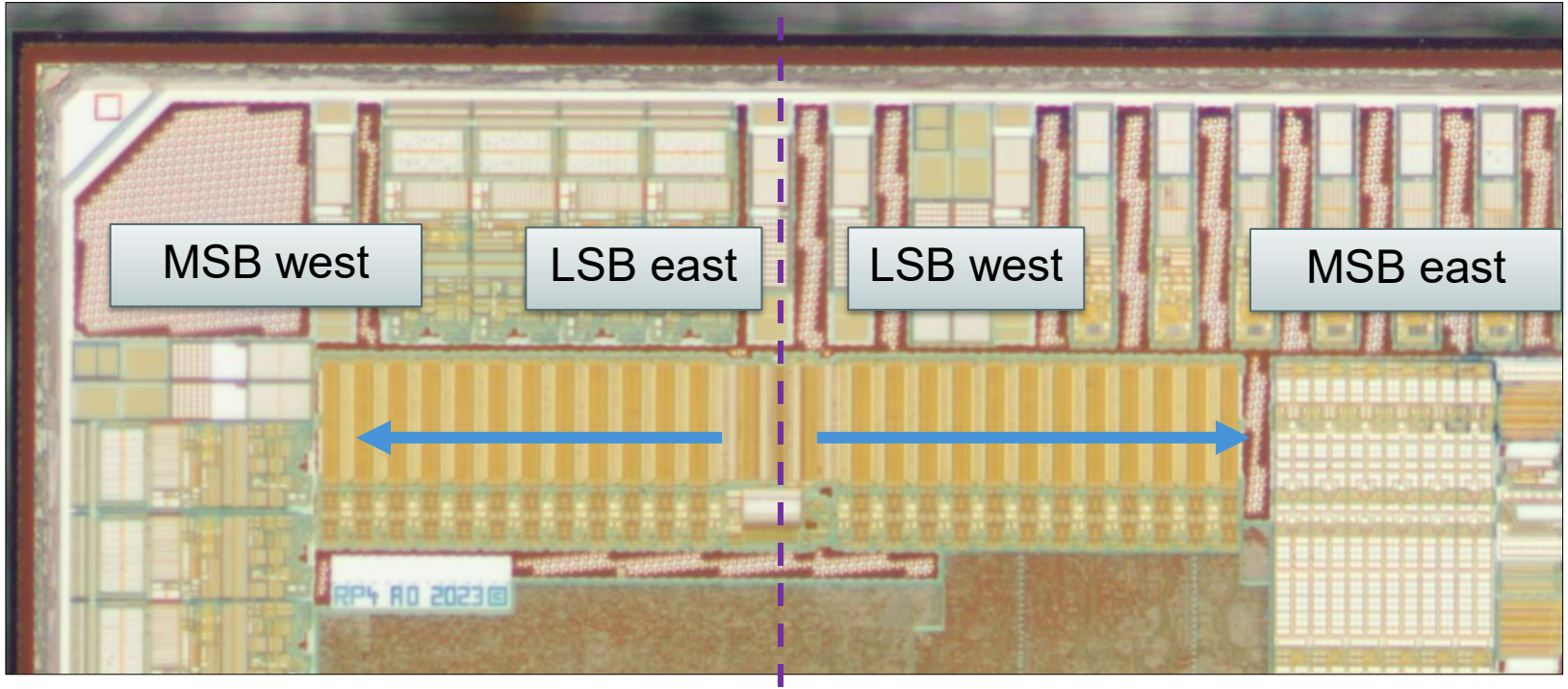







IOActive.

# Bit plane mirroring








IOActive.

# Fuse rendering script

- Python script: fuse values in, ASCII art map out





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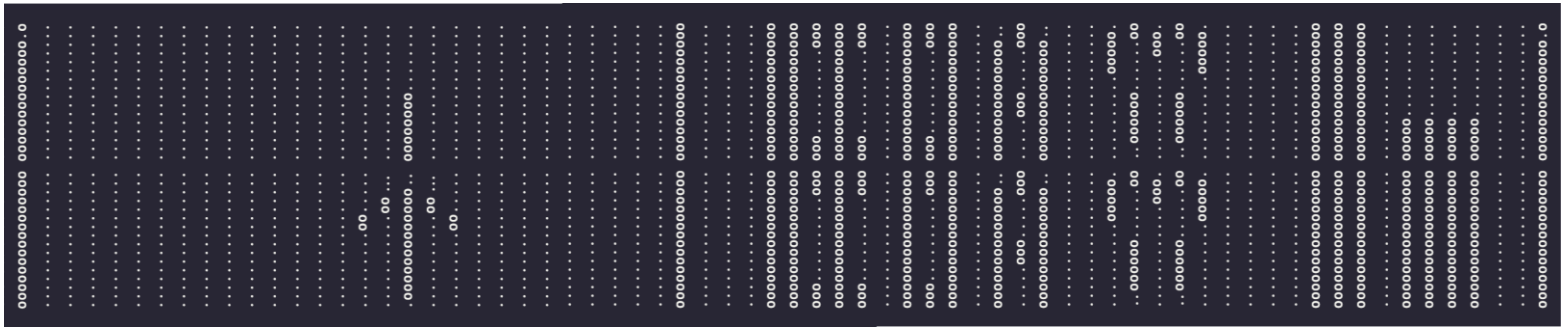
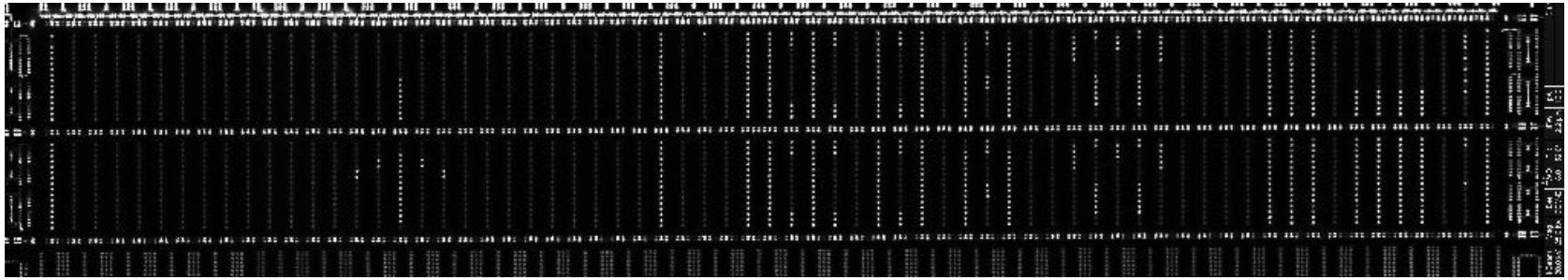
# Full bitplane extraction test









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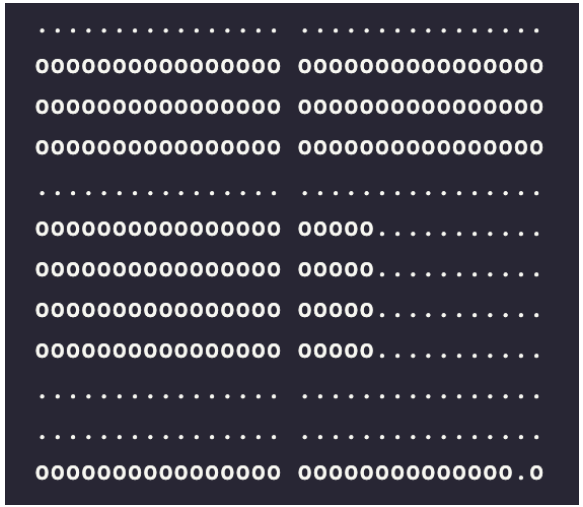
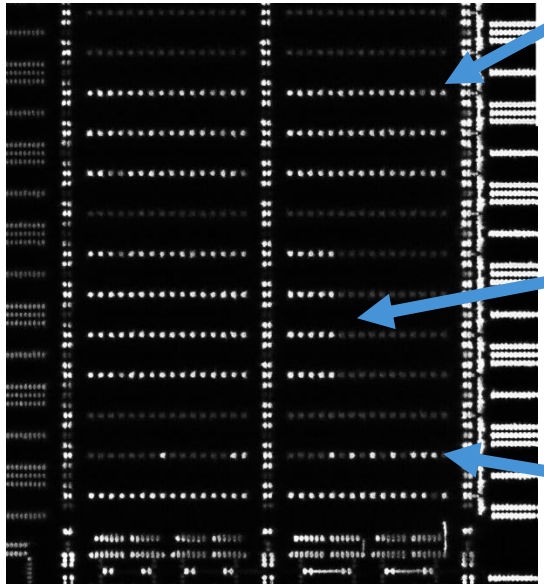
# Test pattern closeup



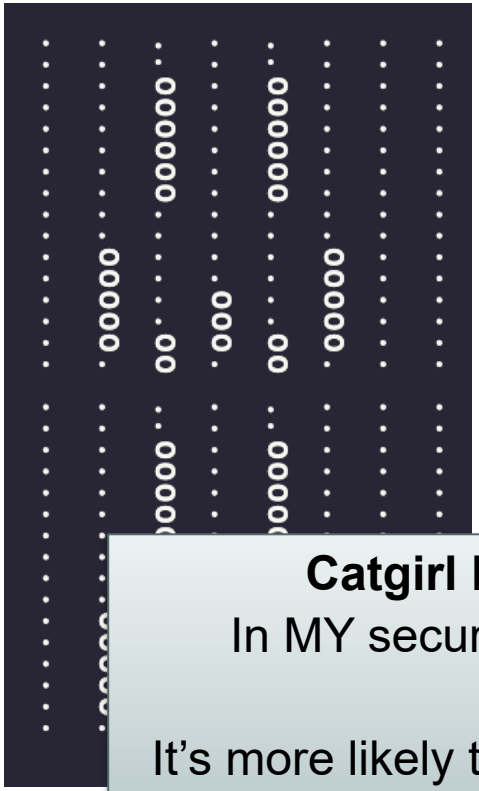



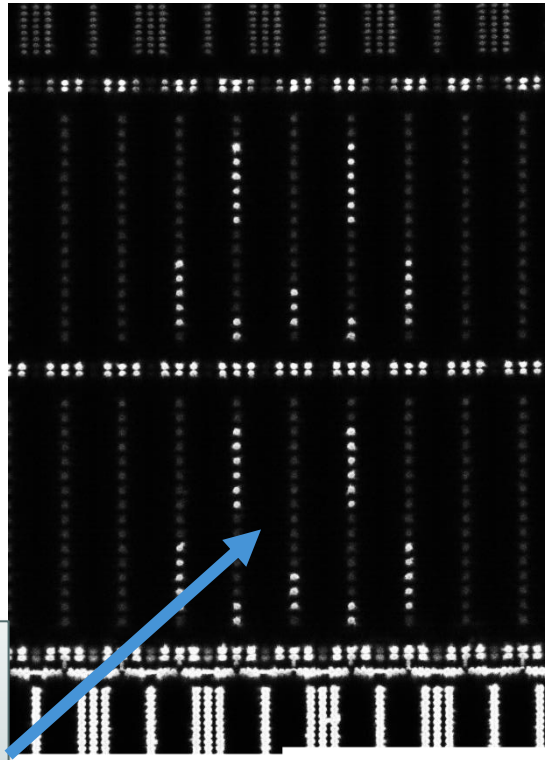





IOActive.

# Test pattern closeup



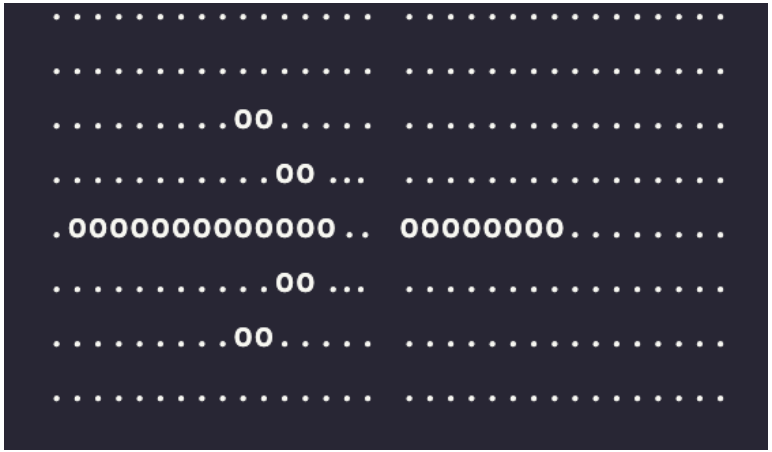


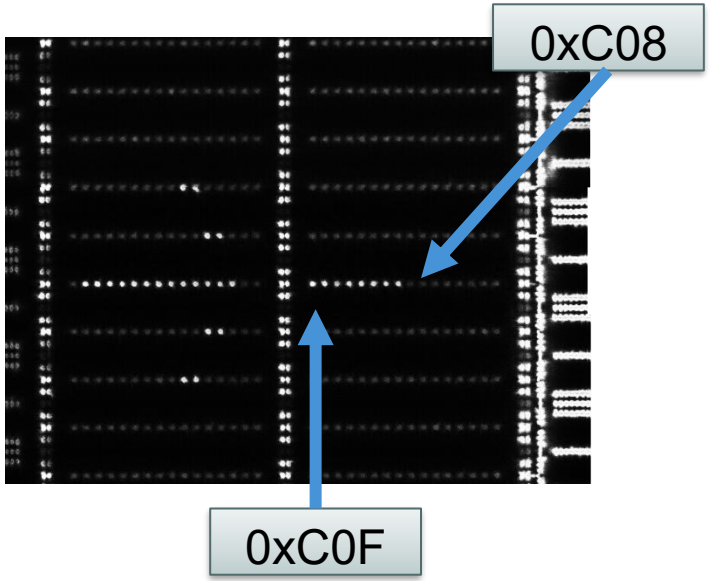
**Catgirl hackers?**

In MY secure boot keys?

It’s more likely than you think =3

# Test pattern closeup






The goal is easy: Find an attack that lets you dump a secret hidden in OTP ROW 0xc08 - the secret is 128-bit long, and protected by `OTP_DATA_PAGE48_LOCK1` and RP2350's secure boot!





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# Possible improvements

- Use probe or FIB platinum to ground half the WLs
  - Should allow readout of even / odd halves separately
  - First experiment failed, haven't had time to try again
- Play w/ scan speed and reduced area scans
  - Bias everything –ve with e-beam
  - Then scan I-beam over WL (to charge) and BL (to image)
  - Make sure not to get *any* beam energy on the opposite WL
  - If perfectly focused, *might* work

# Mitigations

- PVC is physics, impossible to prevent
- Proper fix (requires silicon spin)
  - Encrypt data at rest so fuse dump is worthless to attacker
  - Force adversary to RE many Mgates to find hardwired key
- Near term: increase adversary workload
  - Store 0xFF or ~key in opposite half of paired fuses
  - Blocks the trivial mass-readout attack
  - Requires more work to dump one WL at a time

# Mitigations

- Spread key across many physical words
  - 1 word in N pages is Nx the work to dump vs data in same page
  - Store data all over the place and hash or XOR down
- Goal: force a FIB edit of ~all 2048 WLs in the fuse array
  - Can’t quite use 100% of rows because factory trim etc
  - But you can make the adversary hate you!

# Conclusions

- Antifuses aren’t as invisible as claimed
- A few k$ of FIB time goes a long way
- Any secret in on chip memory can and will be extracted
- Encrypting / obfuscating fuse data raises the bar

# Acknowledgements


- Daniel Slone, Mario Cop, Tony Moor (IOA)
  - Decap, deprocessing, some imaging
- Lain Agan (IOA)
  - Memory map RE, 3D renders, analysis script
- Entropic Engineering
  - RP2350s were hard to find right after launch, they hooked us up
- Raspberry Pi
  - For inviting the hacker community to pwn their product

# Questions?