
AutoLock: Why Cache Attacks on ARM Are Harder Than You Think

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The Big Picture

Cache Attacks

Transition of attacks:
desktop & server → mobile



AutoLock

Dedicated countermeasures
are still necessary for protection

Vulnerability and risk assessment
are important, but challenging



Eviction-based attacks are
harder than previously believed

Limited understanding of
commercial microarchitectures

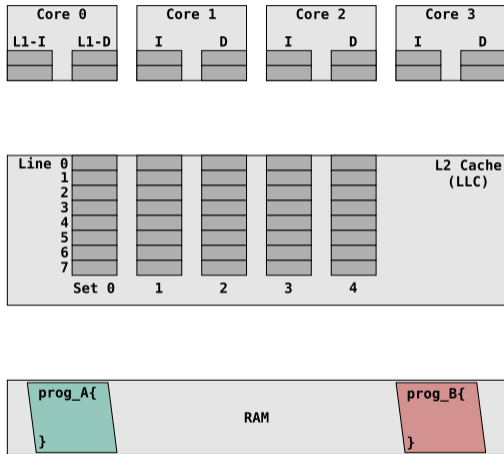


Undocumented performance
feature of inclusive caches on ARM

Cache Basics

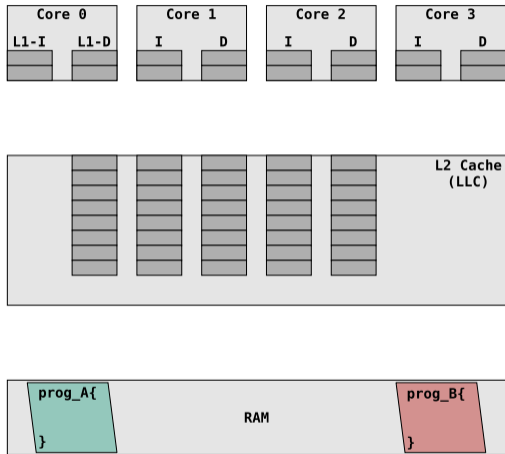
Cache Basics

Hierarchy



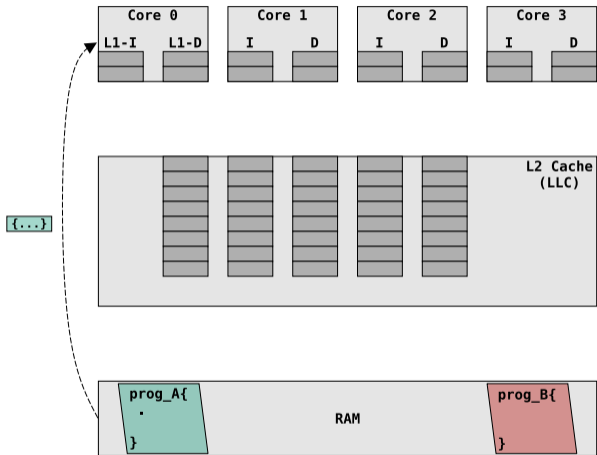
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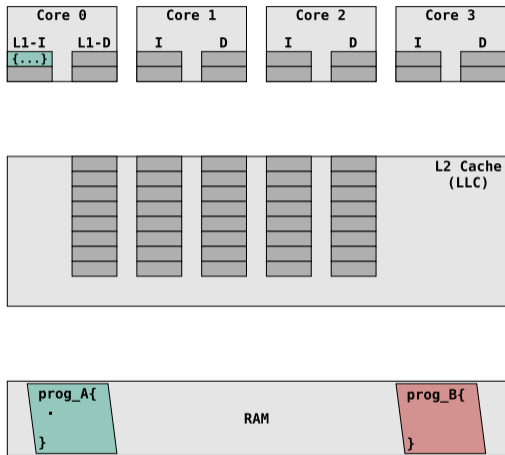
Cache Basics

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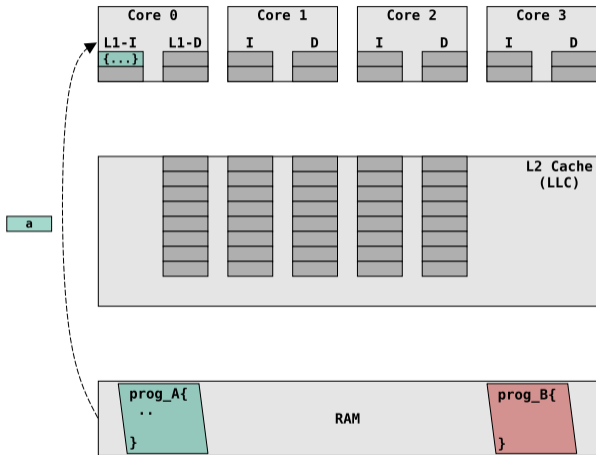
Cache Basics

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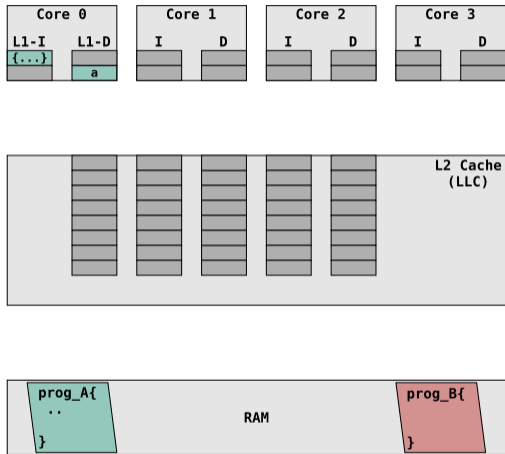
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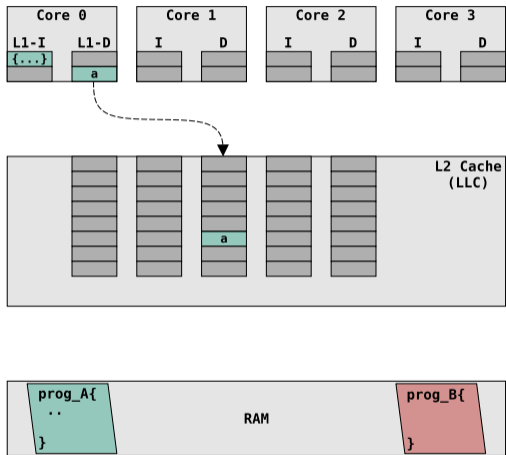
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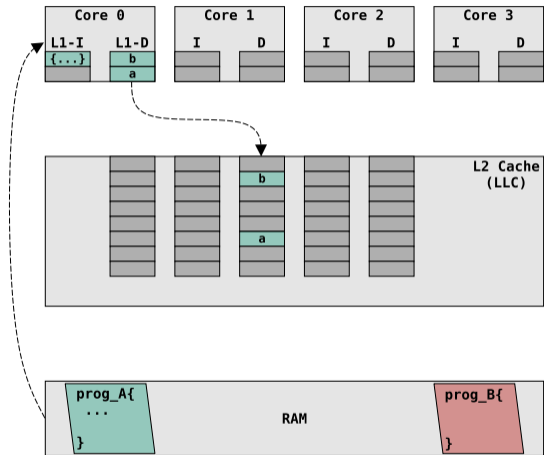
Cache Basics

Inclusiveness



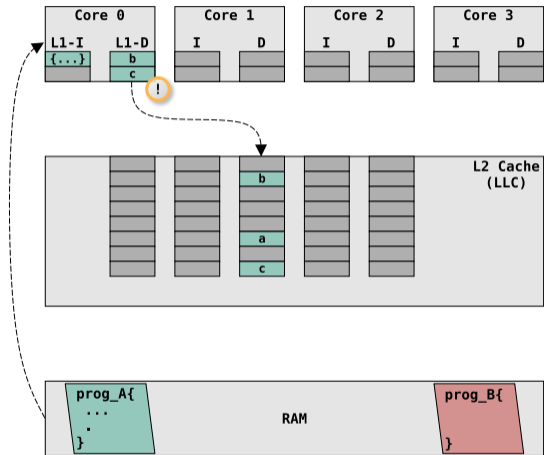
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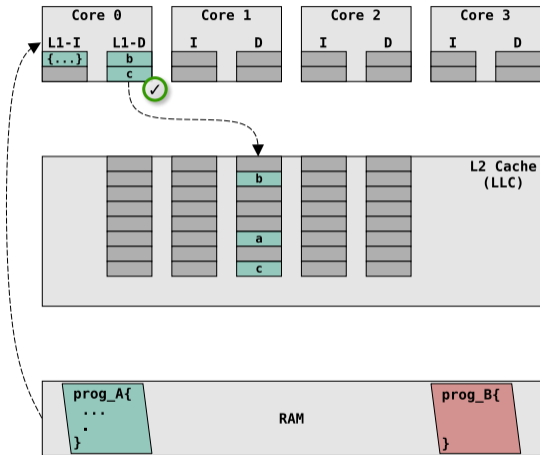
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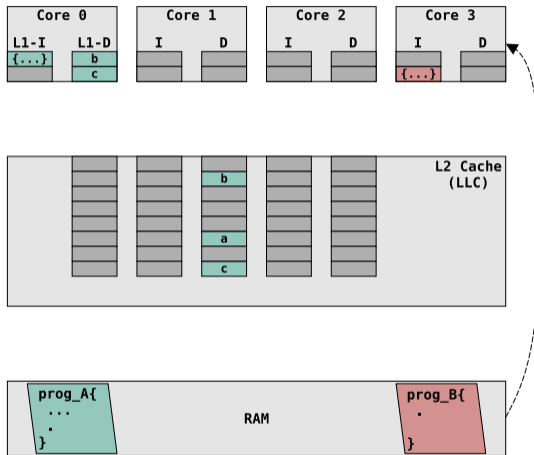
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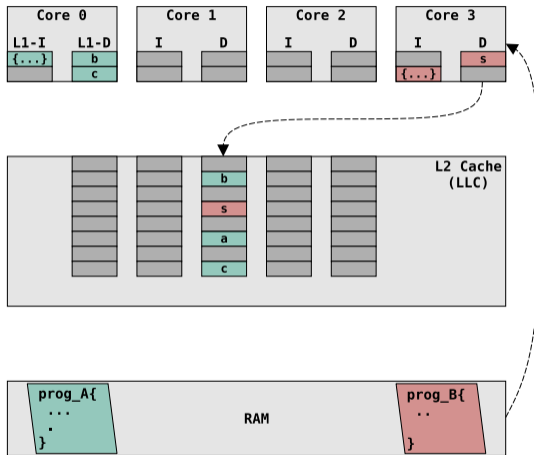
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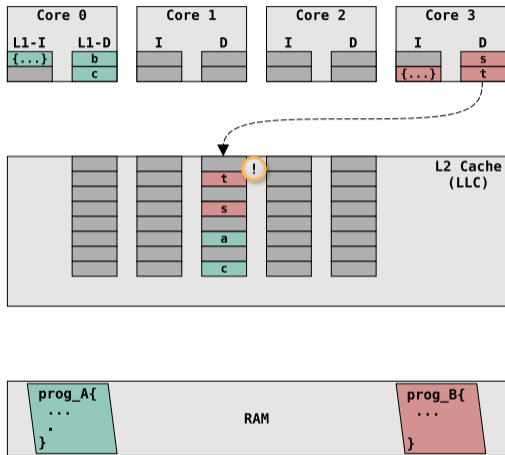
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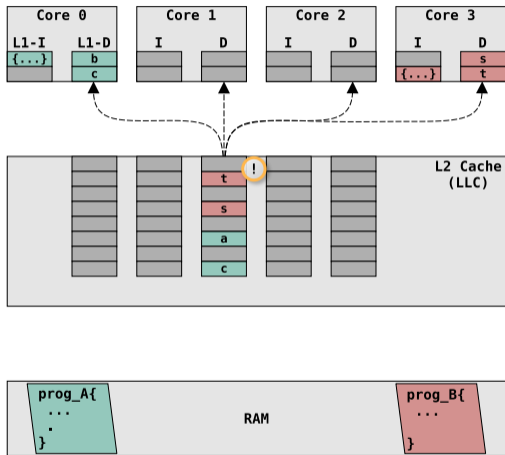
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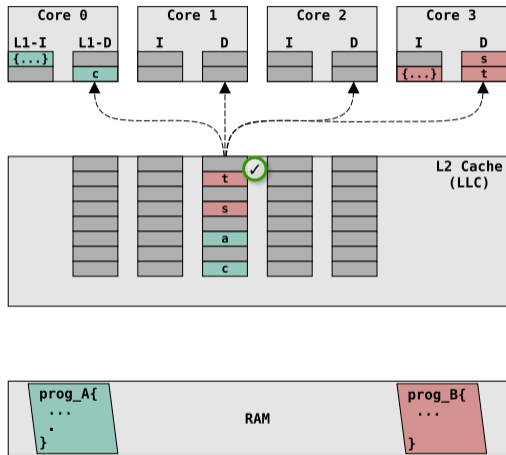
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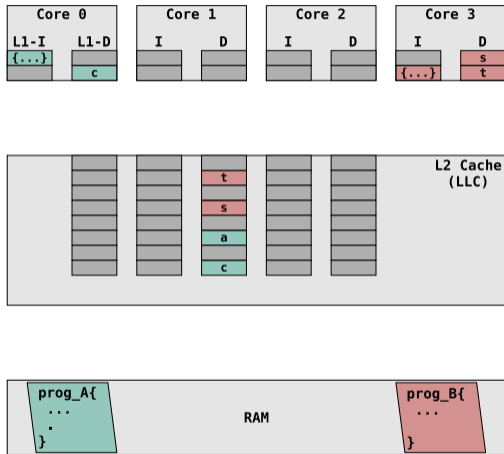
Inclusiveness



Cache Attacks

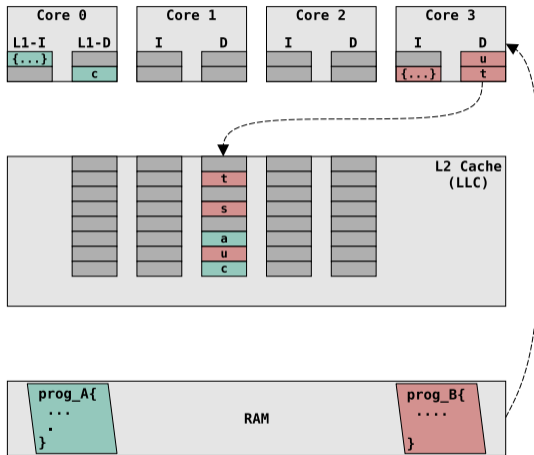
Cache Attacks

Cross-core Eviction



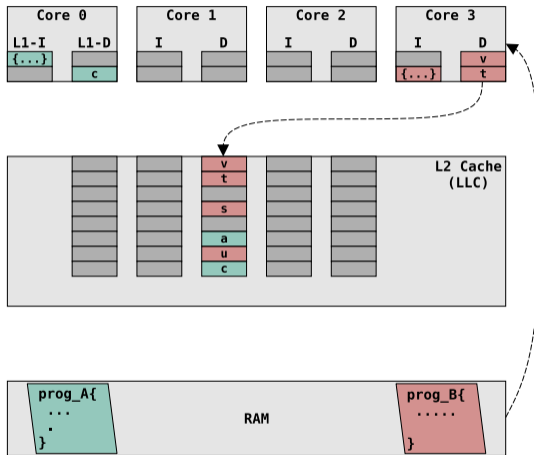
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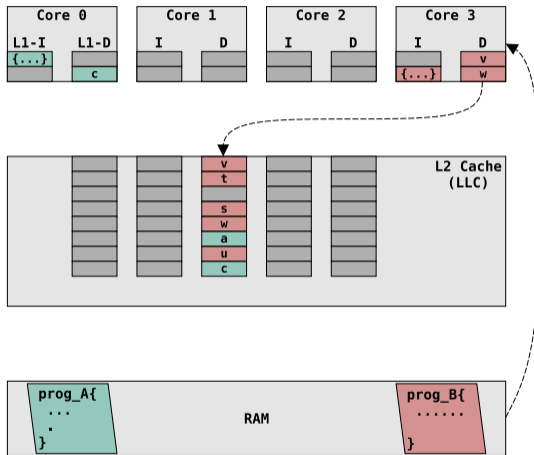
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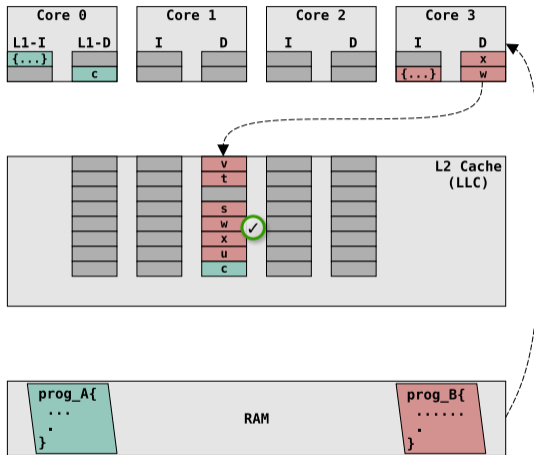
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Cross-core Eviction



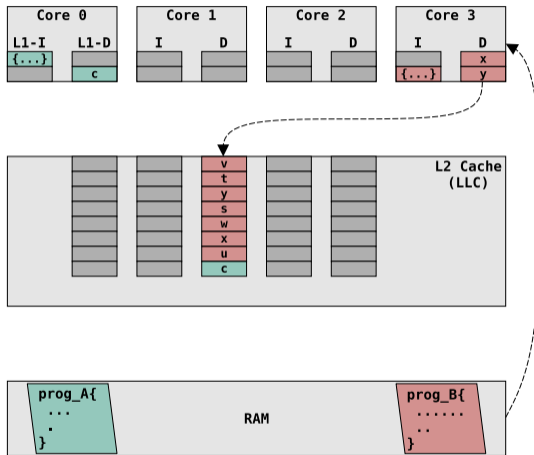
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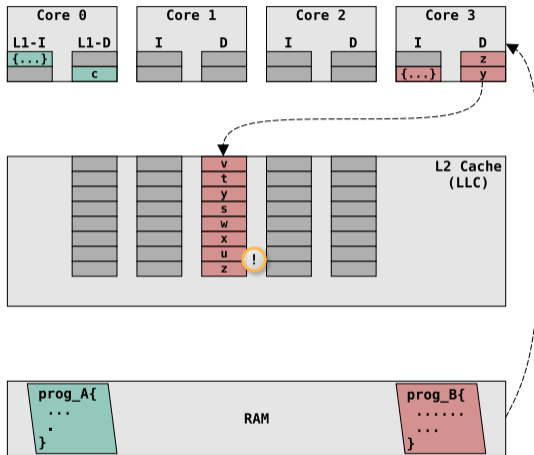
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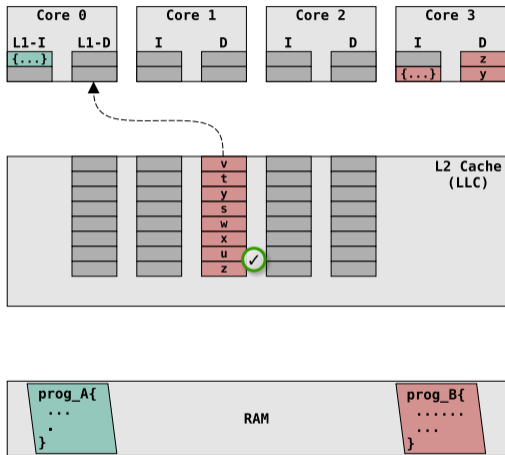
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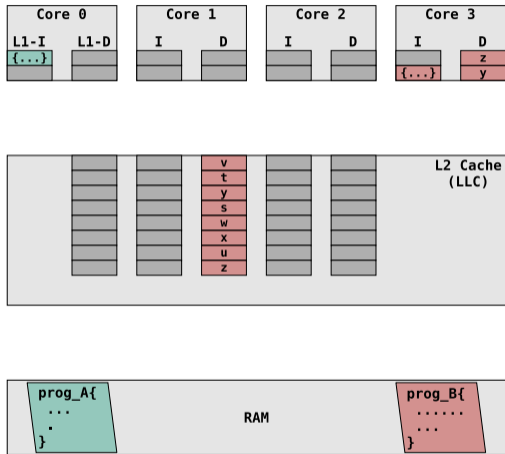
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Cross-core Eviction



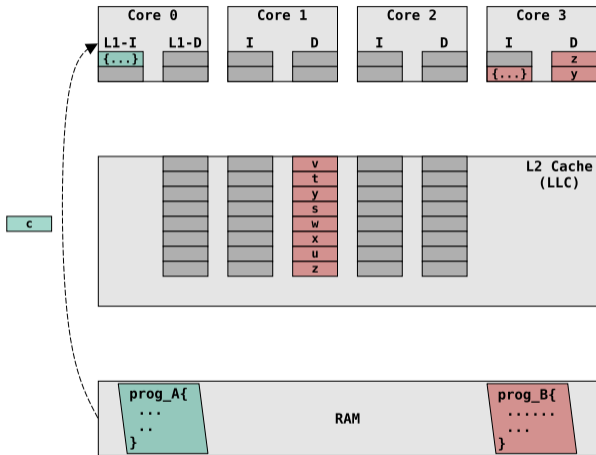
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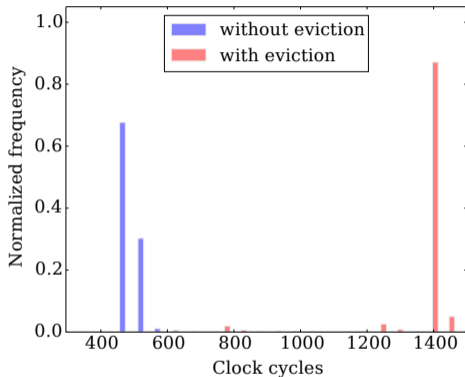
Cache Attacks

Cross-core Eviction



Cache Attacks

Cross-core Eviction



Qualcomm Krait 450

Cache Attacks

Literature

Method	Task	Reference
Evict + Time	Eviction	[OST06]
Prime + Probe	Eviction	[OST06]
Evict + Reload	Eviction	[GSM15]
Evict + Prefetch	Eviction	[GMF ⁺ 16]
Flush + Reload	Flush	[YF14]
Flush + Prefetch	Flush	[GMF ⁺ 16]
Flush + Flush	Flush	[GMWM16]

Flush on ARM

- Easy, fast, and robust
- Only from ARMv8 onwards
- No guaranteed userspace access

Limited number of devices

Eviction on ARM

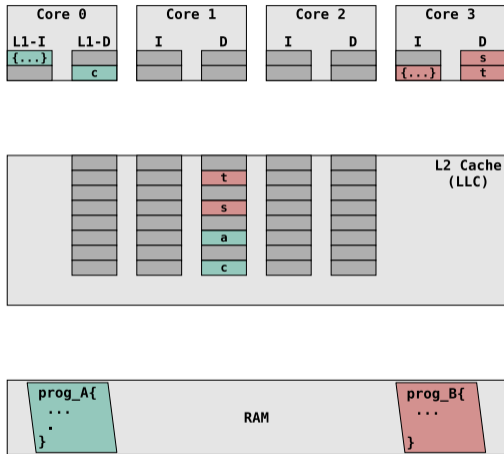
- Complex, slow, and error-prone
- All ARM architectures: v6, v7, v8
- Userspace privileges are sufficient

Larger number of devices

AutoLock

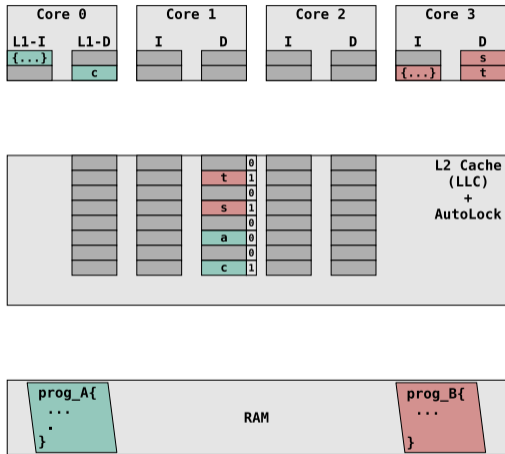
AutoLock

Cross-core Eviction



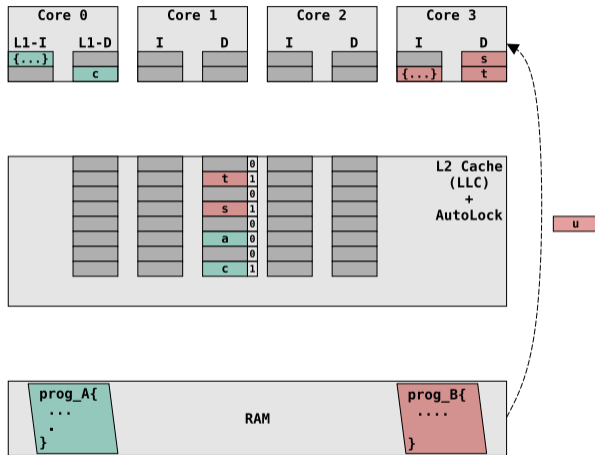
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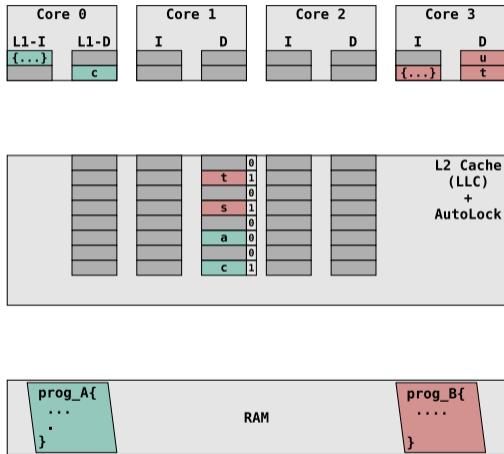
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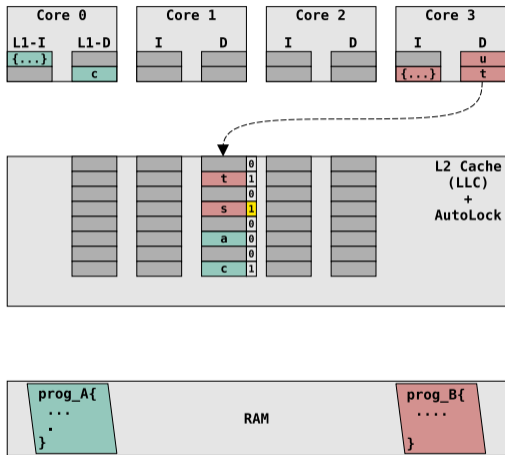
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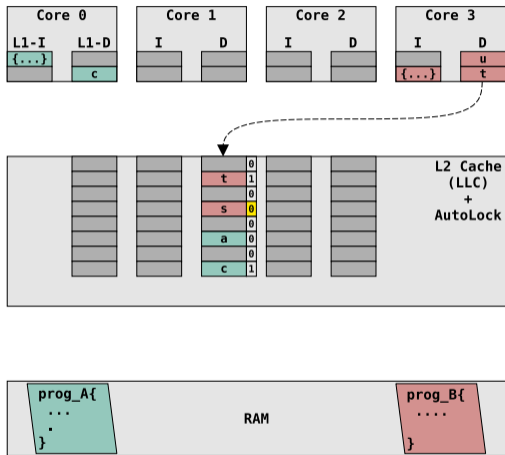
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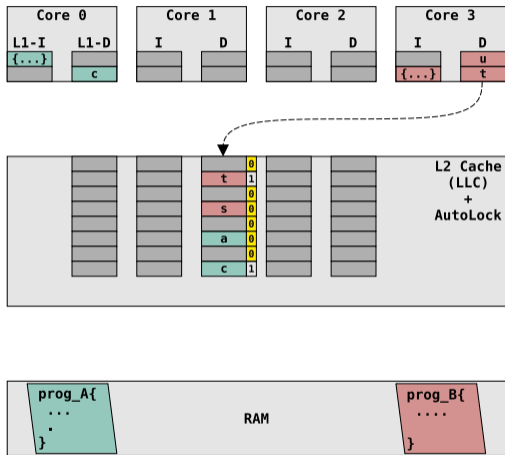
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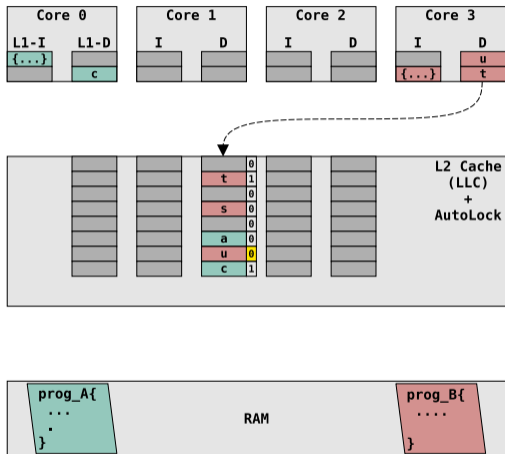
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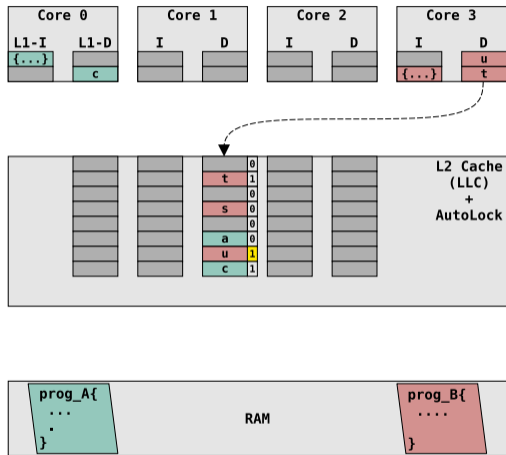
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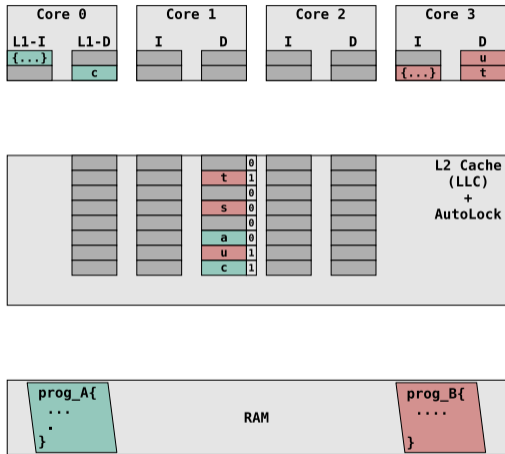
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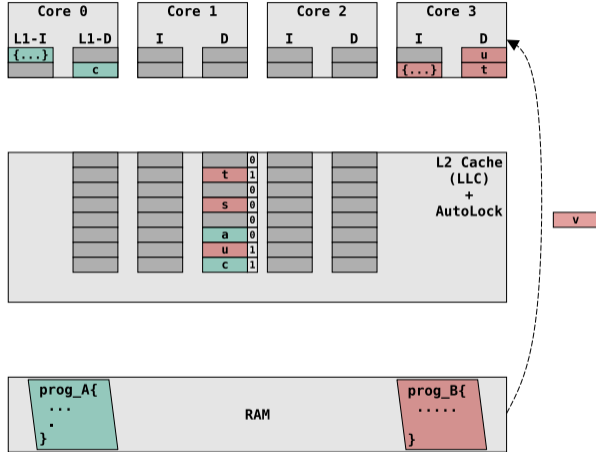
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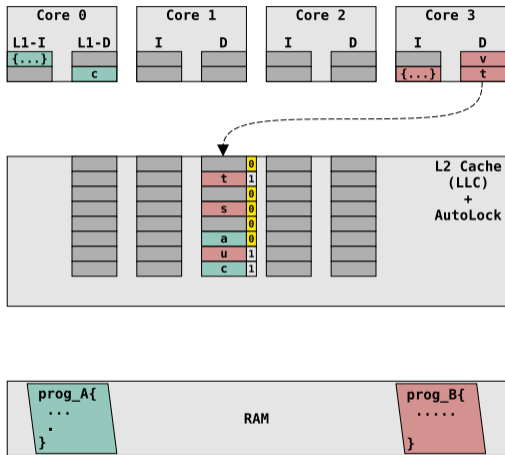
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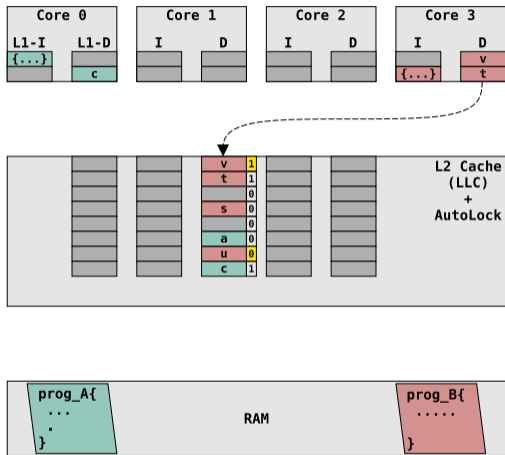
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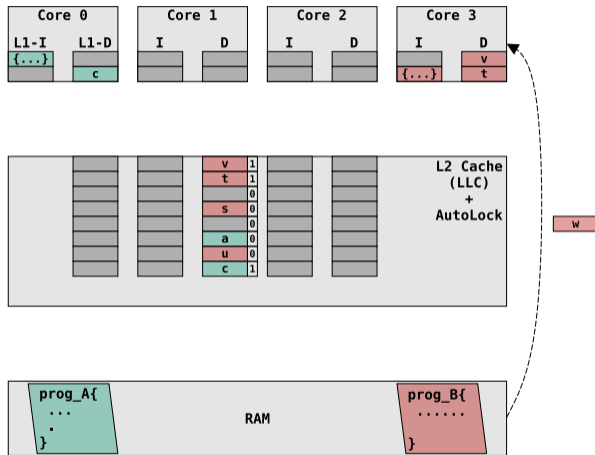
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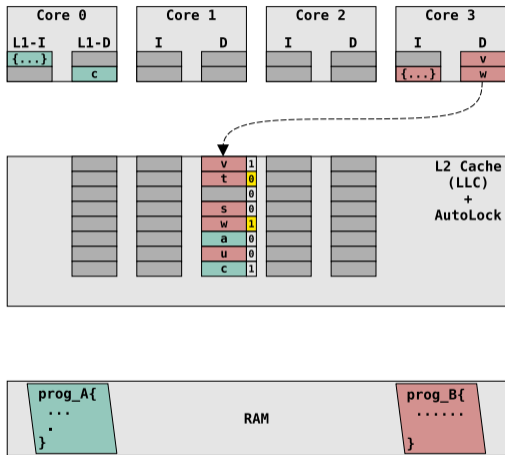
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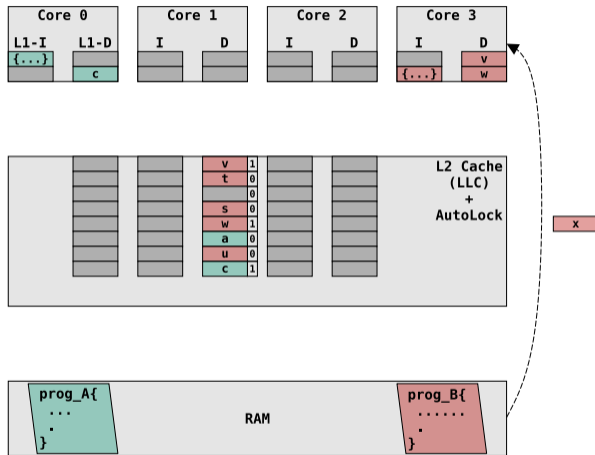
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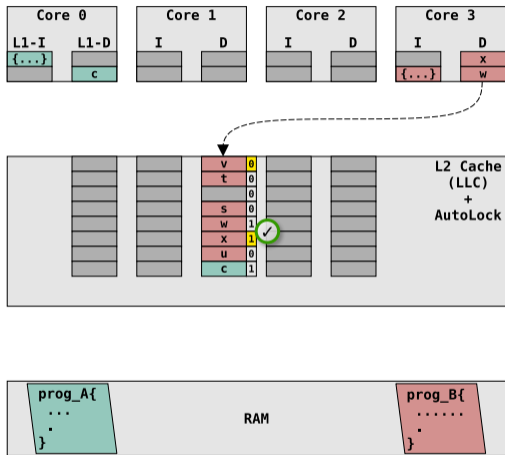
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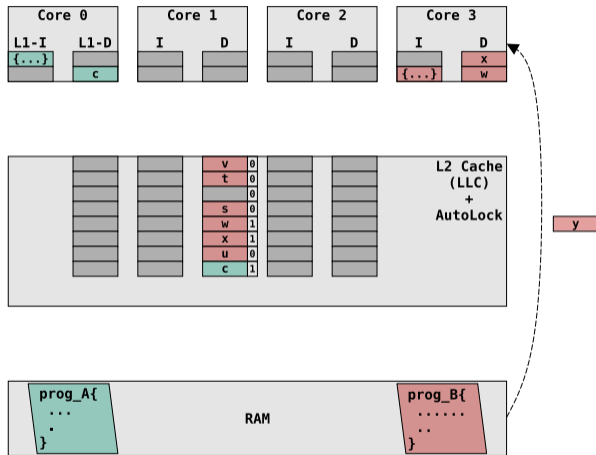
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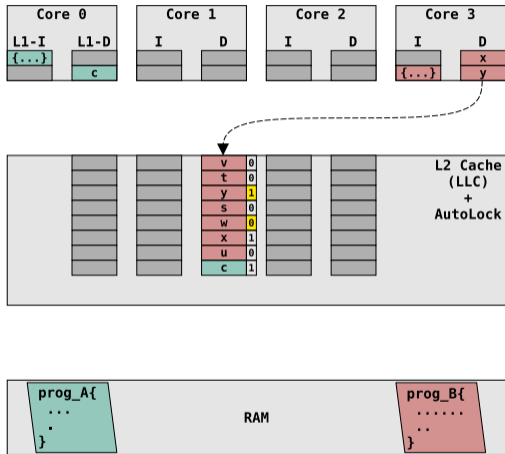
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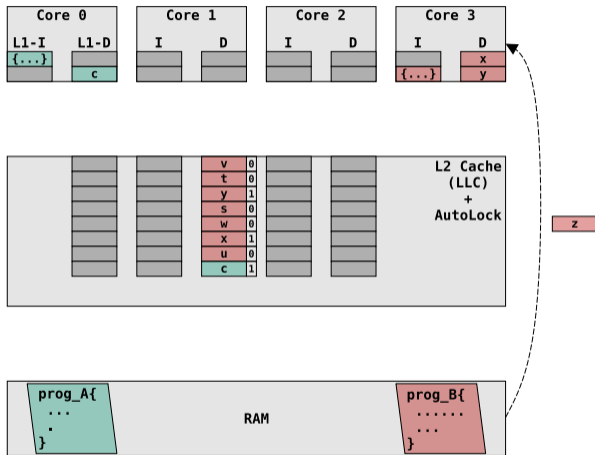
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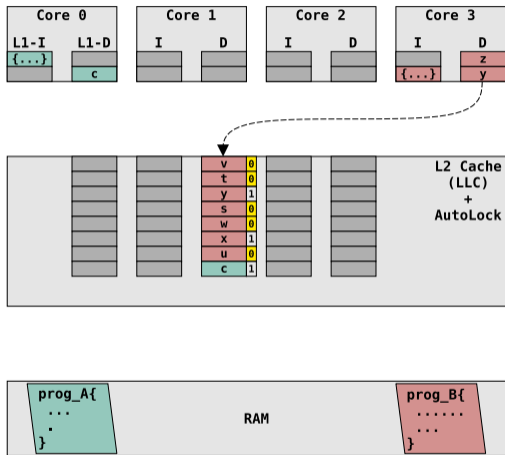
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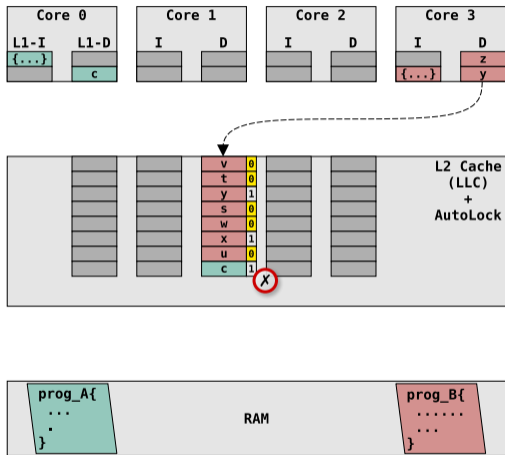
AutoLock

Cross-core Eviction



AutoLock

Cross-core Eviction



AutoLock

Definition

A patented and undocumented performance feature of inclusive cache levels that transparently prevents the eviction of cache lines, if they are contained in higher cache levels.

Automatic + Lockdown = "AutoLock"

Implications of AutoLock

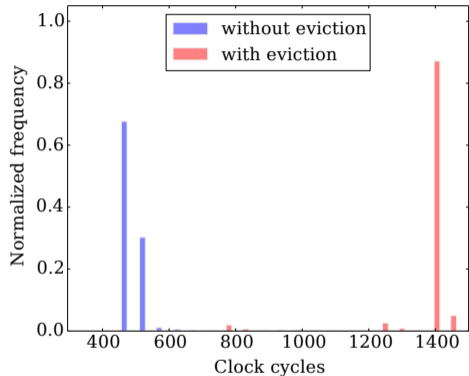
Implications

Impact in Theory

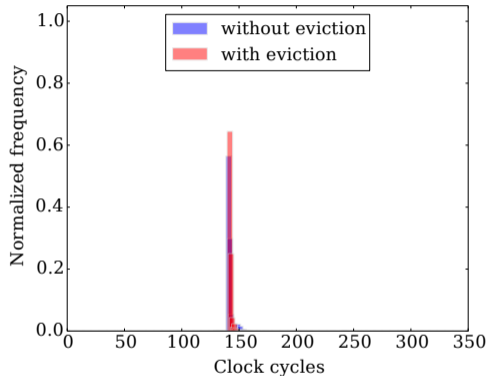
Method	Task	Same-core	Cross-core
Evict + Time	Eviction	✓	✗
Prime + Probe	Eviction	✓	✗
Evict + Reload	Eviction	✓	✗
Evict + Prefetch	Eviction	✓	✗
Flush + *	Flush	✓	✓

Implications

Impact in Practice



Qualcomm Krait 450



ARM Cortex-A57

Implications

SoC Evaluation

Processor	System-on-Chip (SoC)	AutoLock
ARM Cortex-A7	Samsung Exynos 5422	✓
ARM Cortex-A15	Samsung Exynos 5422/5250	✓
ARM Cortex-A53	ARM Juno r0	✓
ARM Cortex-A57	ARM Juno r0	✓
Qualcomm Krait 450	Snapdragon 805	✗

Implications

Smartphone SoCs

Manufacturer	SoC Family	% featuring A7,-15,-53,-57
Apple	A10, A9, A8, A7	0
HiSilicon	Kirin 9xx, 6xx	86
Mediatek	MT67xx, MT659x/8x	100
Nvidia	Tegra X, K, 4	71
Qualcomm	Snapdragon 8xx, 6xx, 4xx	47
Samsung	Exynos 9, 8, 7, 5, 4	79
Xiaomi	Surge S	100

Implications

Previous Work on ARM

"ARMageddon"

Lipp et al. [LGS⁺16]

⇒ Device Selection

- Qualcomm SoCs
- Userspace flush
- Cross-core eviction

"ROP Flush + Reload"

Zhang et al. [ZXZ16]

⇒ Attack Selection

- Flush + Reload
- `cacheflush` syscall
- No cross-core eviction

"TruSpy"

Zhang et al. [ZSS⁺16]

⇒ Device Properties

- ARM Cortex-A8
- Single-core setup
- No cross-core eviction

AutoLock = Countermeasure?

Countermeasure?

Not Ultimately

Vulnerable SoCs

- ARM-compliant cores
- Userspace flush instr.

Remote Evictions

- Trigger self-evictions
- Increase load and wait time

Same-Core Attacks

- ARM TrustZone
- Compromised OS

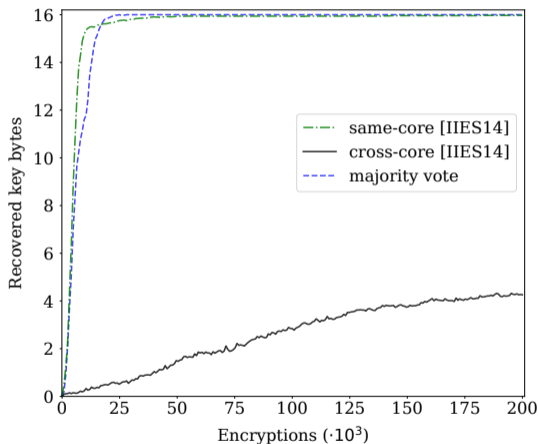
Redundant Targets

- Attack multiple cache lines
- e.g. entire AES T-tables

Countermeasure?

Wait-a-minute Attack

- Attack by Irazoqui et al. [IIES14]
 - Observes usage of AES T-tables
 - One cache line per table
- Simple redundant variant
 - Observe all lines of all tables
 - Majority vote on derived keys
- Test environment
 - ARM Cortex-A15 with `AutoLock`
 - Full Linux operating system



Conclusion

Conclusion

Takeaways

AutoLock: undocumented feature of inclusive LLCs on ARM

Inhibits cross-core eviction and adversely affects attacks

Predominantly implemented in Cortex-A designs by ARM

Countermeasures are still necessary to protect against attacks

Questions ?

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