Optimizing NAND Flash-Based SSDs via Retention Relaxation

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### Motivation

- **Retention specification vs. actual retention requirement**
  - Industrial standards: 1 to 10 years vs. Applications’ needs: days or shorter

- **Retention relaxation**
  - If we don’t need to guarantee the maximal retention time, which design parameters of SSDs can be improved?

- **Contribution**
  - We propose retention-aware designs to trade data retention for the benefits on write speed, or ECCs’ cost and performance

### NAND Flash Model

- **Threshold voltage (Vth) distribution model**
  - Probability density function of cells’ Vth
  - $P_k(V_t) = \alpha_k \exp \left( -\frac{V_t - \mu_k}{\sigma_k} \right)$, $k = 0$
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- **Raw bit error rate (RBER)**
  - $RBER(t) = \sum_{k=0}^{K} \exp \left( -\frac{V_t - \mu_k}{\sigma_k} \right)$

### Benefits of Retention Relaxation

- **Improving write speed**
  - Enlarging the step increment ($\Delta V_p$) in NAND Flash’s programming procedures
  - Reduction decreases because the $V_{th}$ distributions become wider and the margins between neighboring levels get narrower
  - Write speed increases because with large $\Delta V_p$, fewer programming steps are required during writes
  - 2.3x write speedup is achievable if data retention is reduced to 2 weeks

- **Improving ECCs’ cost and performance**
  - Advanced ECCs such as LDPC codes are required for NAND Flash whose bit error rate $\geq 10^{-3}$
  - Shorter retention guarantee → fewer retention errors → less required ECC strength
  - BCH is strong enough for NAND Flash with the bit error rate up to $2.2 \times 10^{-2}$ if the retention guarantee is relaxed to 2 weeks

### System Evaluation

- **SSD write response time speedup**
  - Retention Relaxation achieves 2.2x to 5.5x speedup
  - Hadoop has the largest speedup
  - High I/O throughput and long queuing time
  - Retention Relaxation significantly reduces the queuing time

- **SSD performance vs. various LDPC throughput**
  - Retention Relaxation outperforms the baseline (conventional concatenated BCH-LDPC) with the same LDPC throughput
  - Retention Relaxation approaches the ideal performance with 20MB/s LDPC

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*The SSD simulator could stop simulations due to I/O queue saturation if LDPC’s throughput is insufficient. The bar of the baseline presents a yagag appearance between 5~80 MB/s because several traces which cause saturation are excluded.*