**Motivation: Enhanced Reliability for SSDs**

- Problem with current SSDs: low reliability
  - High error rate and limited erase count of flash memory
  - Multi-level cell (MLC) flash memory aggravates problem
- One solution: provide RAID-5 configuration with chips comprising the SSD device

**Problems**

- Typical RAID-5 [Logical Block Number (LBN) based striping]: Parity update burden
  - Small write problem: read old data, calculate parity, write new data
- Added burden when adopting RAID-5 configuration to SSDs: Out-of-place update
  - With LBN-based striping ⇒ MUST keep (new) updated page in SAME chip as old page

- Lower performance & reliability, higher cleaning cost, decreased lifetime

- Our solution: Dynamic Stripping-RAID (DS-RAID)

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**Logical Block Number (LBN) based striping**

- Need Stripe map table in RAID Controller
- Must read old data & old parity
- May result in particular chips being written to more frequently (skewed writes)
- Window of vulnerability for new small writes

**Physical Page Number (PPN) based striping**

- No need for Stripe map table
- No need to read old data & old parity
- All chips are written to evenly
- RAID-5 reliability for new small writes (even without non-volatile RAM)

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**Evaluation Platform and Results**

- **Evaluation platform**
  - SSD Extension for DiskSim
- **Parameter**
  - Number of chips: 8
  - Pages per chip: 8
  - Blocks per plane: 256
  - Pages per block: 64
  - Over provision space: 5%
  - Page size: 4KB
  - Stripe size: 2KB

- **Workload**
  - Postmark: 1.6MB (Avg. write size)
  - Random write: 12KB (Avg. write size)

- **Includes**
  - Parity writes
  - Writes for cleaning
  - Sub-parity stripe writes

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