The Bleak Future of NAND Flash Memory

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Microsoft Research

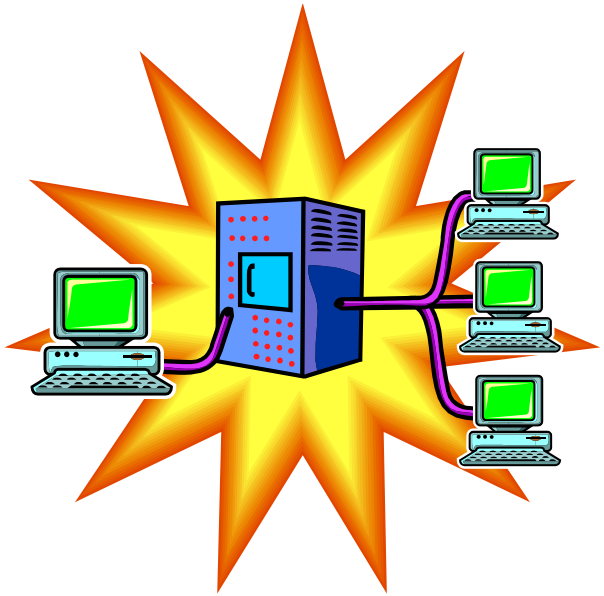
NVSL
Non-volatile Systems Laboratory

UCSDCSE
Computer Science and Engineering

Flash's Future: Bright

Reliability

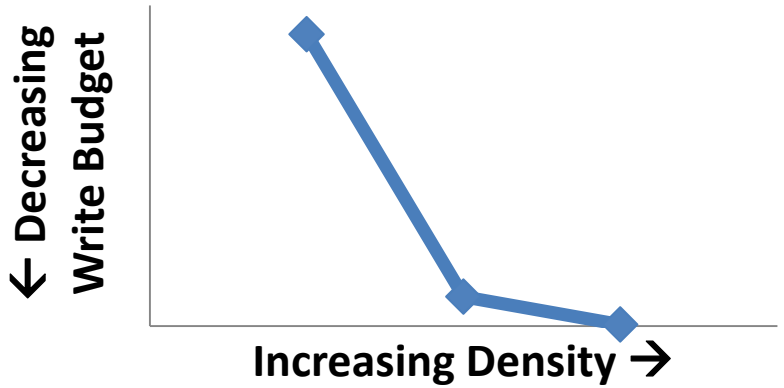
Performance



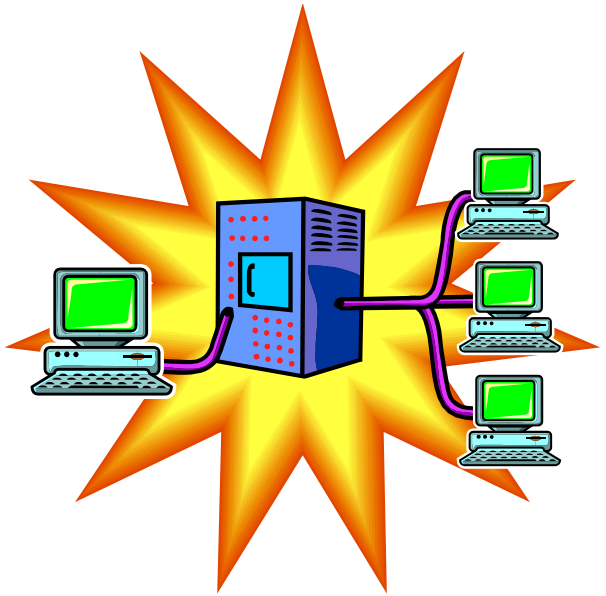
Cost Per Capacity

Flash's Future: ~~Bright~~ Bleak

Reliability



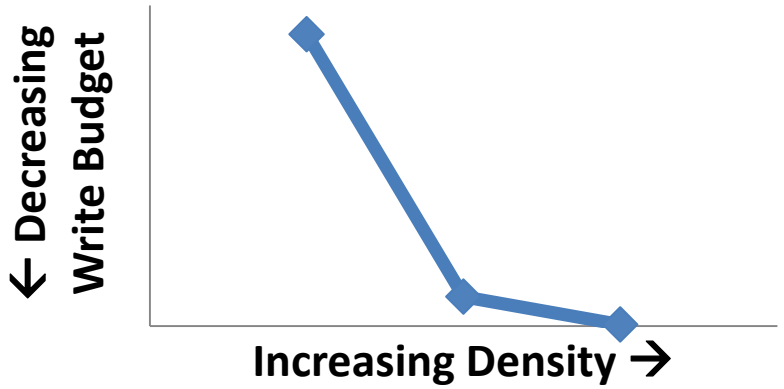
Performance



Cost Per Capacity

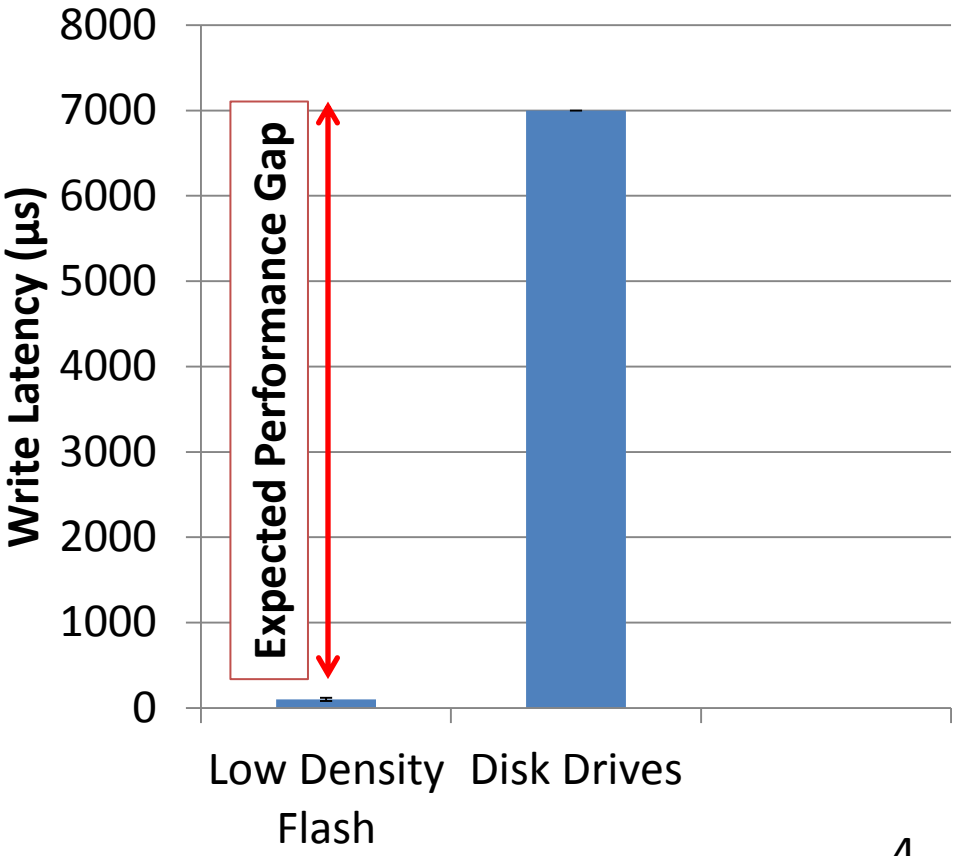
Flash's Future: ~~Bright~~ Bleak

Reliability



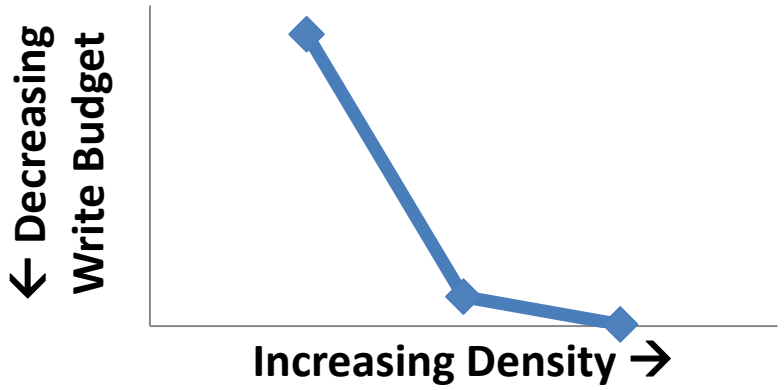
Cost Per Capacity

Performance



Flash's Future: ~~Bright~~ Bleak

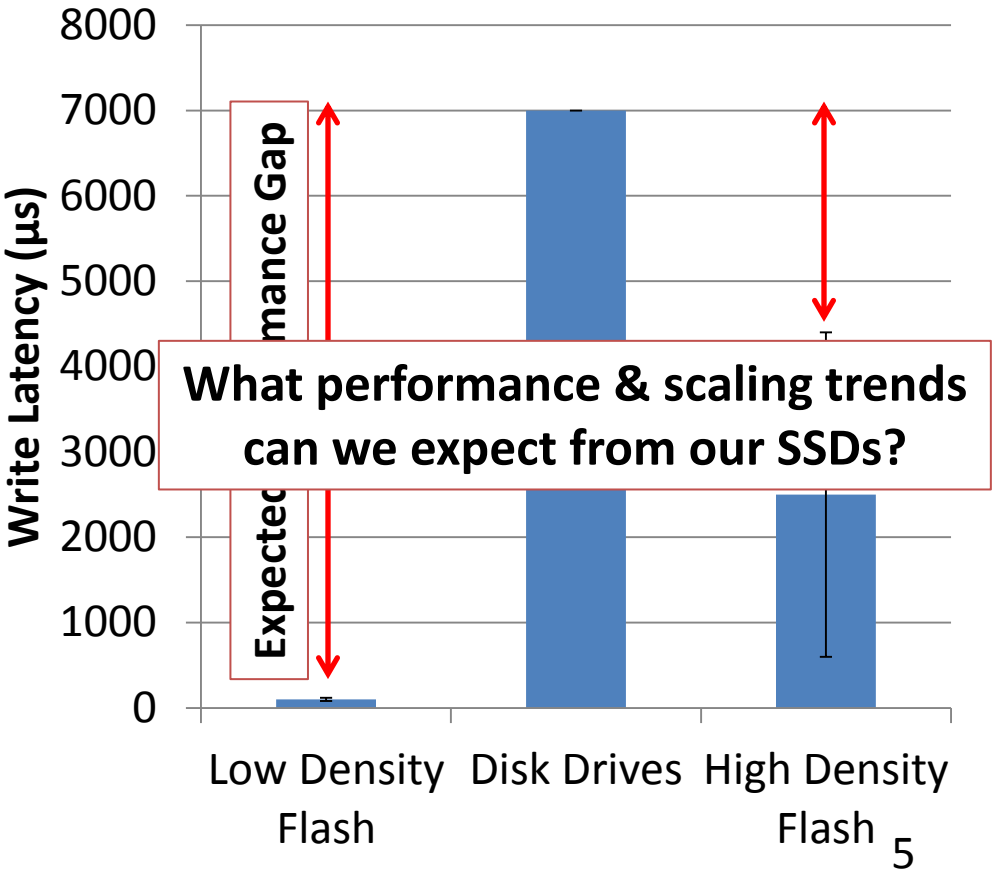
Reliability



Cost Per Capacity

Will the price decline be enough?

Performance

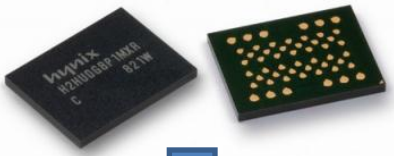


What performance & scaling trends can we expect from our SSDs?

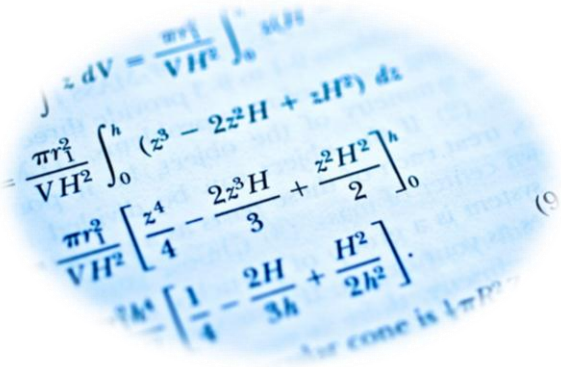
Predicting Future Flash-Based SSDs

Fixed SSD Architecture

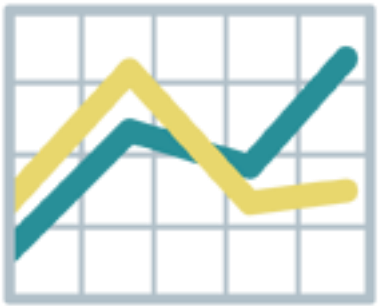
Flash Chip Trends



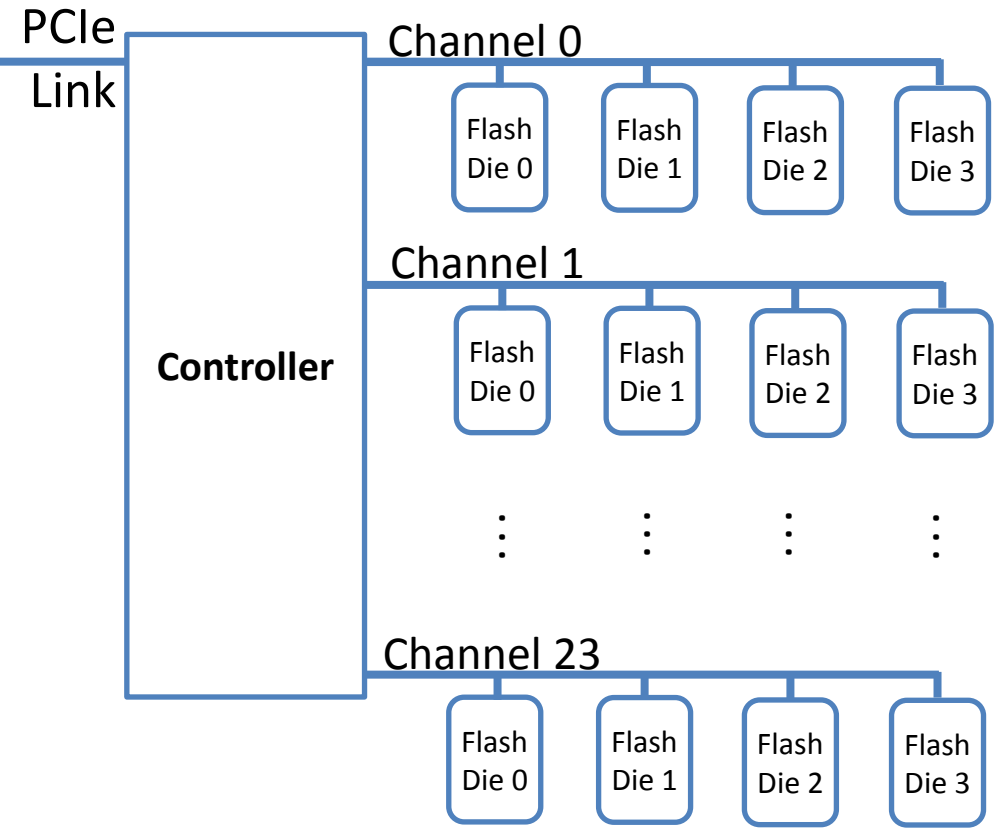
Model's Equations



SSD Trends



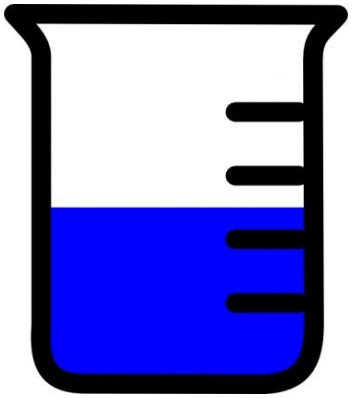
The Constant-Die-Count SSD (SSD-CDC)



- Represents High-End (FusionIO, Virident, OCZ)
- Baseline
  - 96 dies
  - 320 GB
  - 34nm, MLC
- Assumptions
  - Constant die count
  - Unlimited PCIe Link
  - Channel Speed: 400MB/s

The Metrics

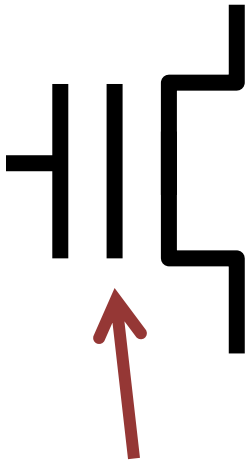
- Capacity



- Latency

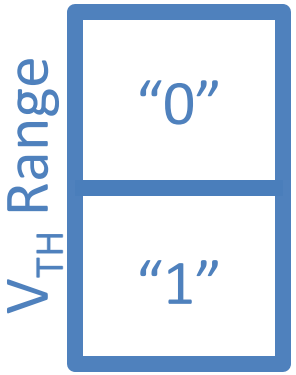
- Throughput

Increasing Density: Multi-bit Cells

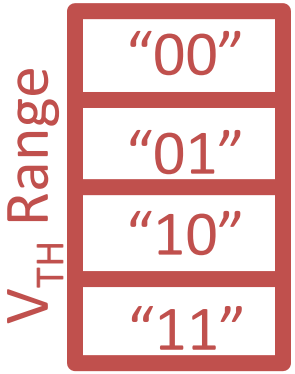


Floating Gate
(modifies V_{TH})

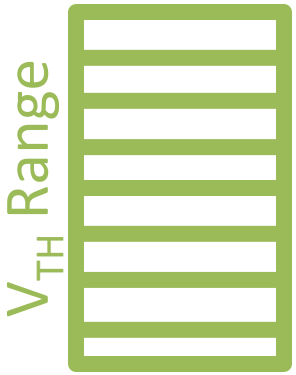
SLC
Single-Level Cell
(1 bit)



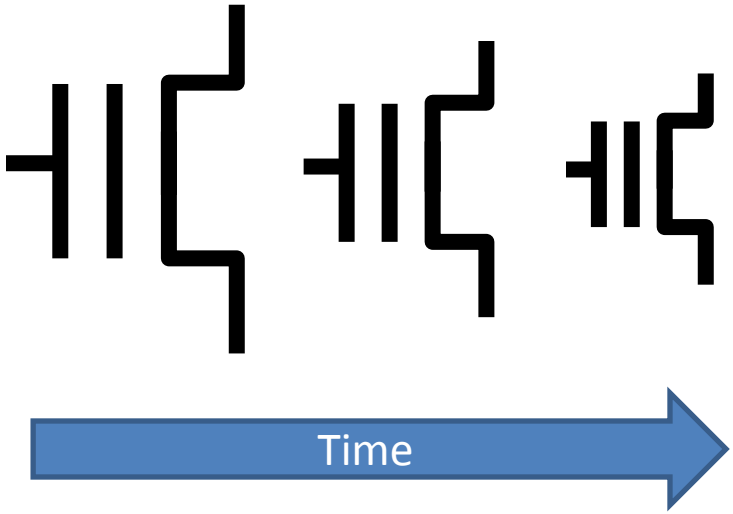
MLC
Multi-Level Cell
(2 bits)

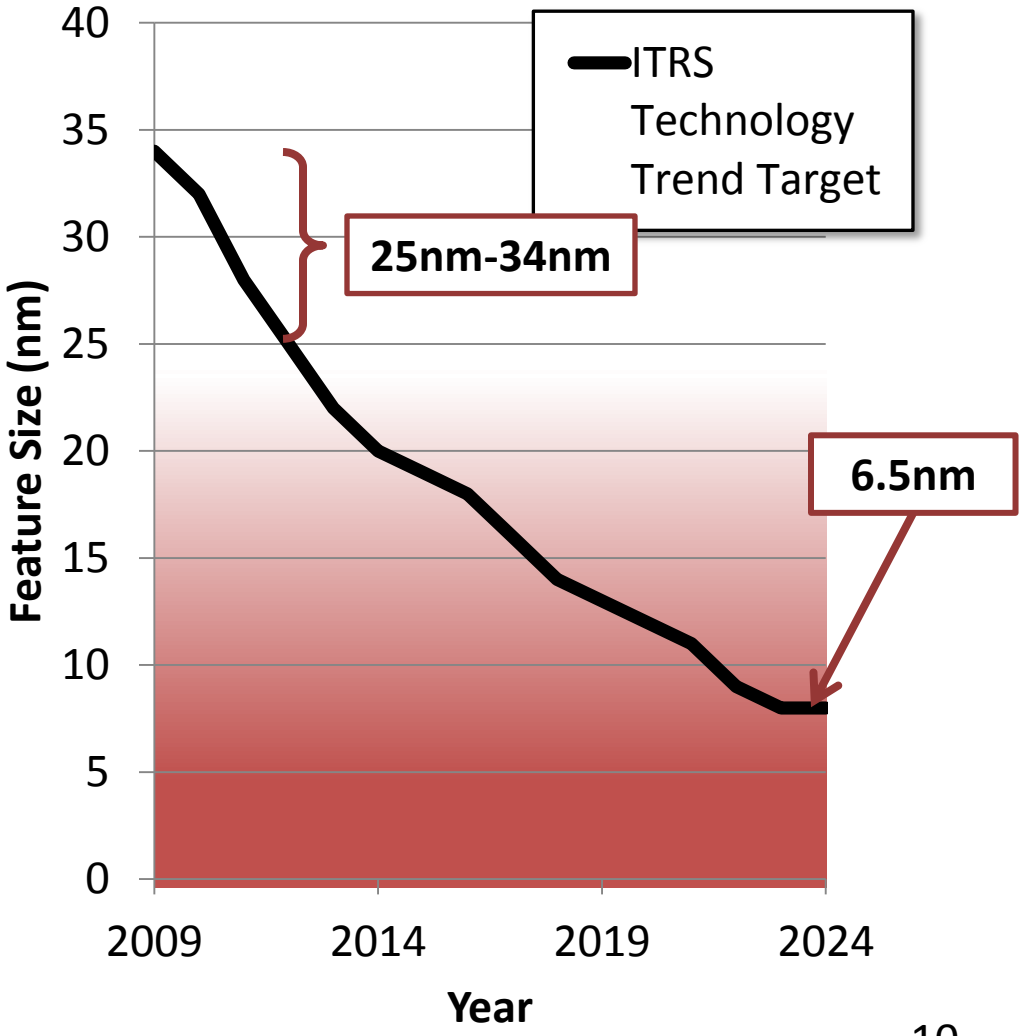


TLC
Triple-Level Cell
(3 bits)

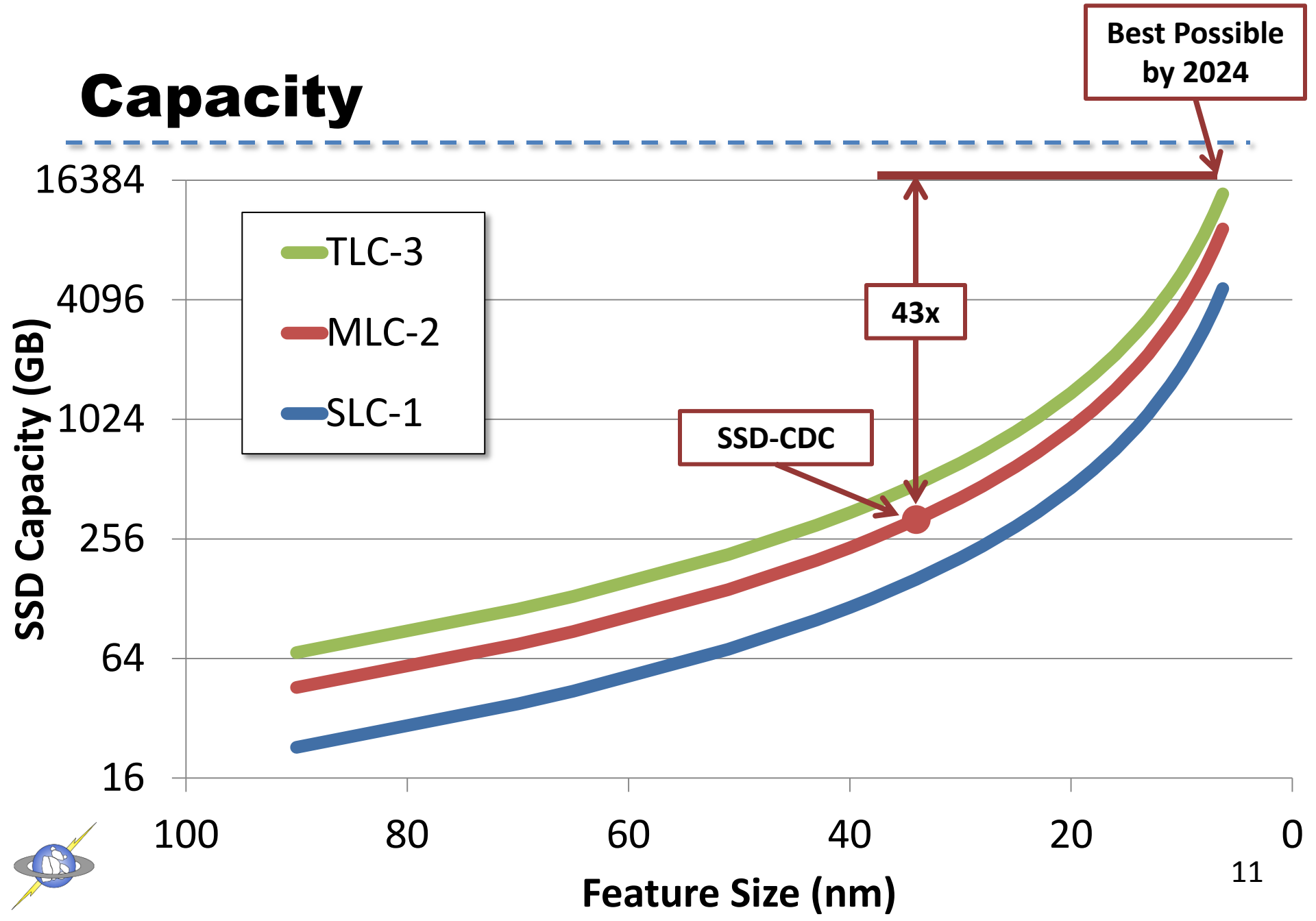


Increasing Density: Moore's Law





Capacity


Best Possible by 2024
43x
SSD-CDC
TLC-3
MLC-2
SLC-1
16384
4096
1024
256
64
16
SSD Capacity (GB)
100
80
60
40
20
0
Feature Size (nm)

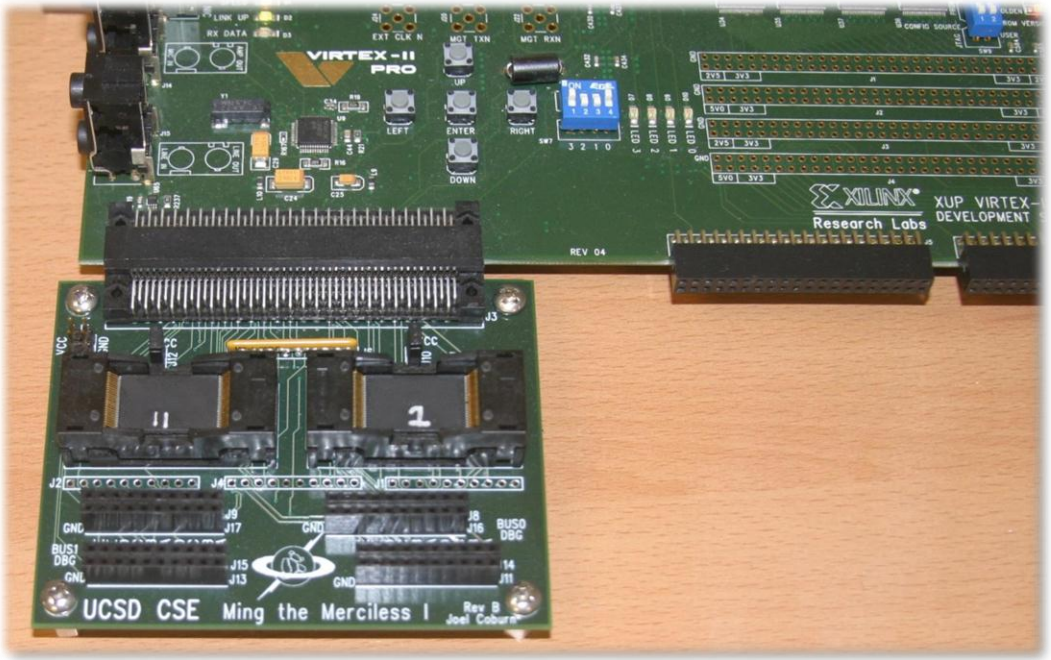
The Metrics

- Capacity: 43x
- Latency

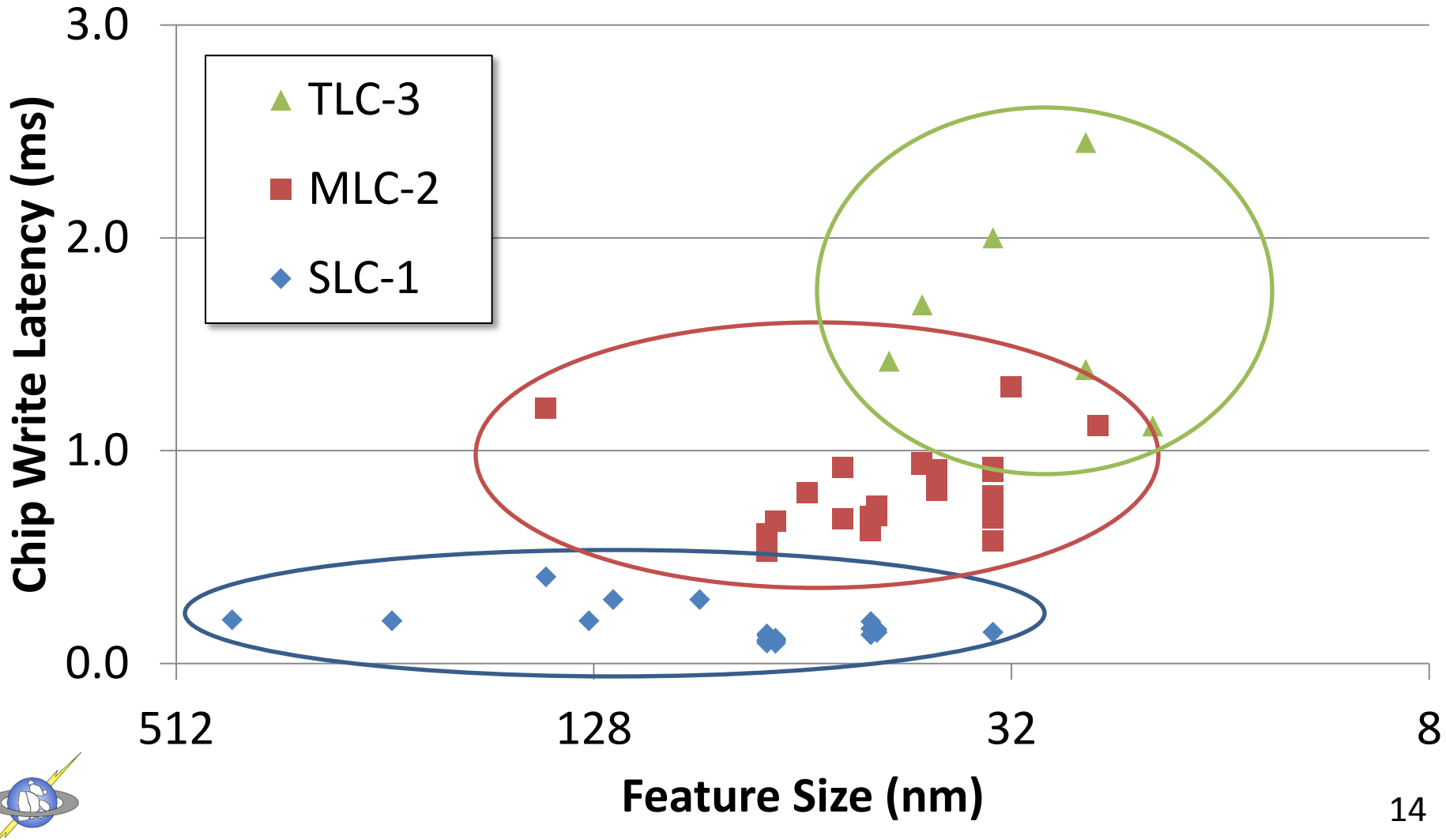
- Throughput

Collecting Flash Latency Trends

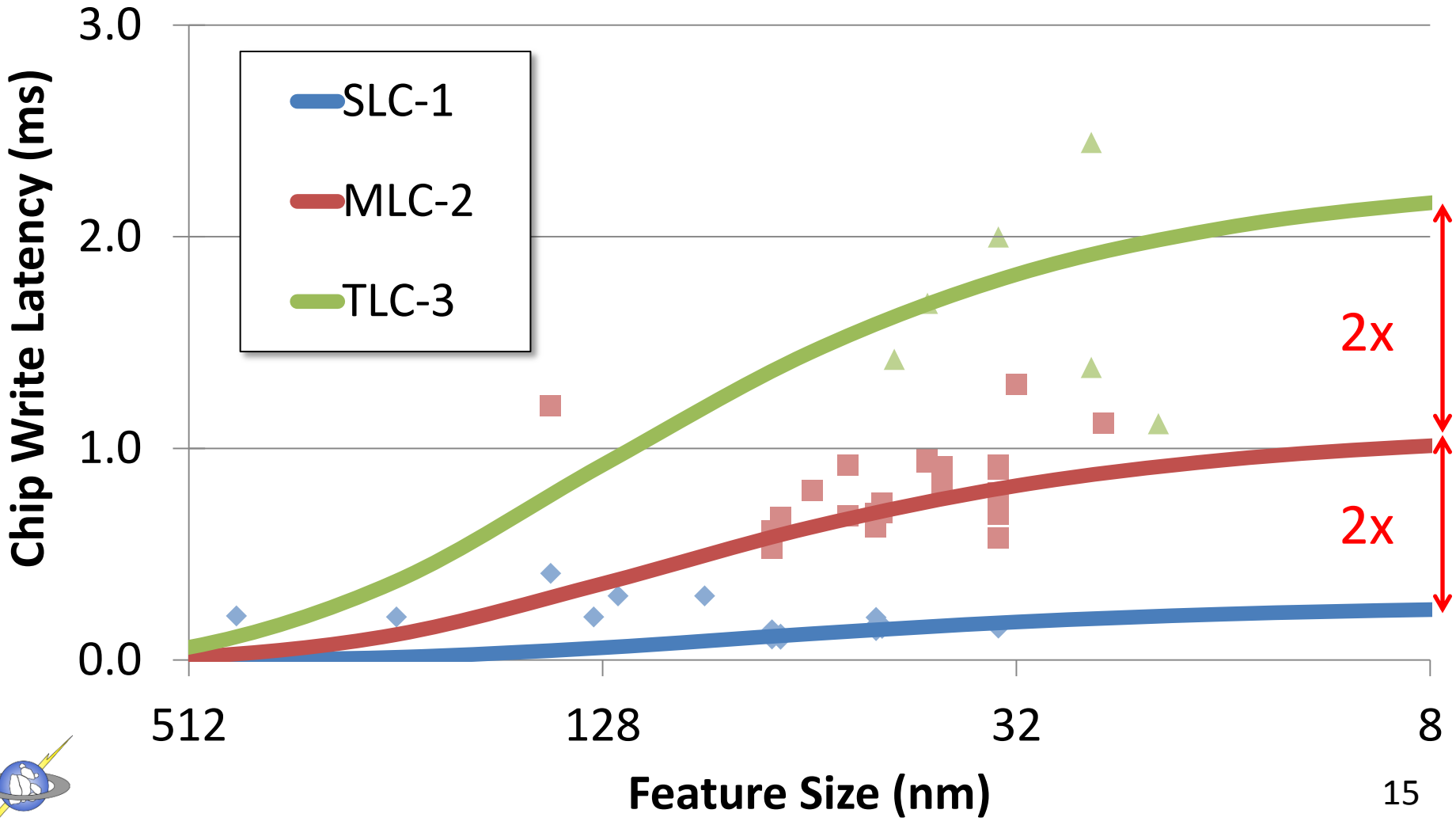
- In-house flash testing rig
  - XUP Virtex-II
  - Daughter board
  - 10ns resolution
- Chip Collection
  - 45 chips
  - 6 companies
  - 25nm-72nm
  - SLC, MLC, TLC



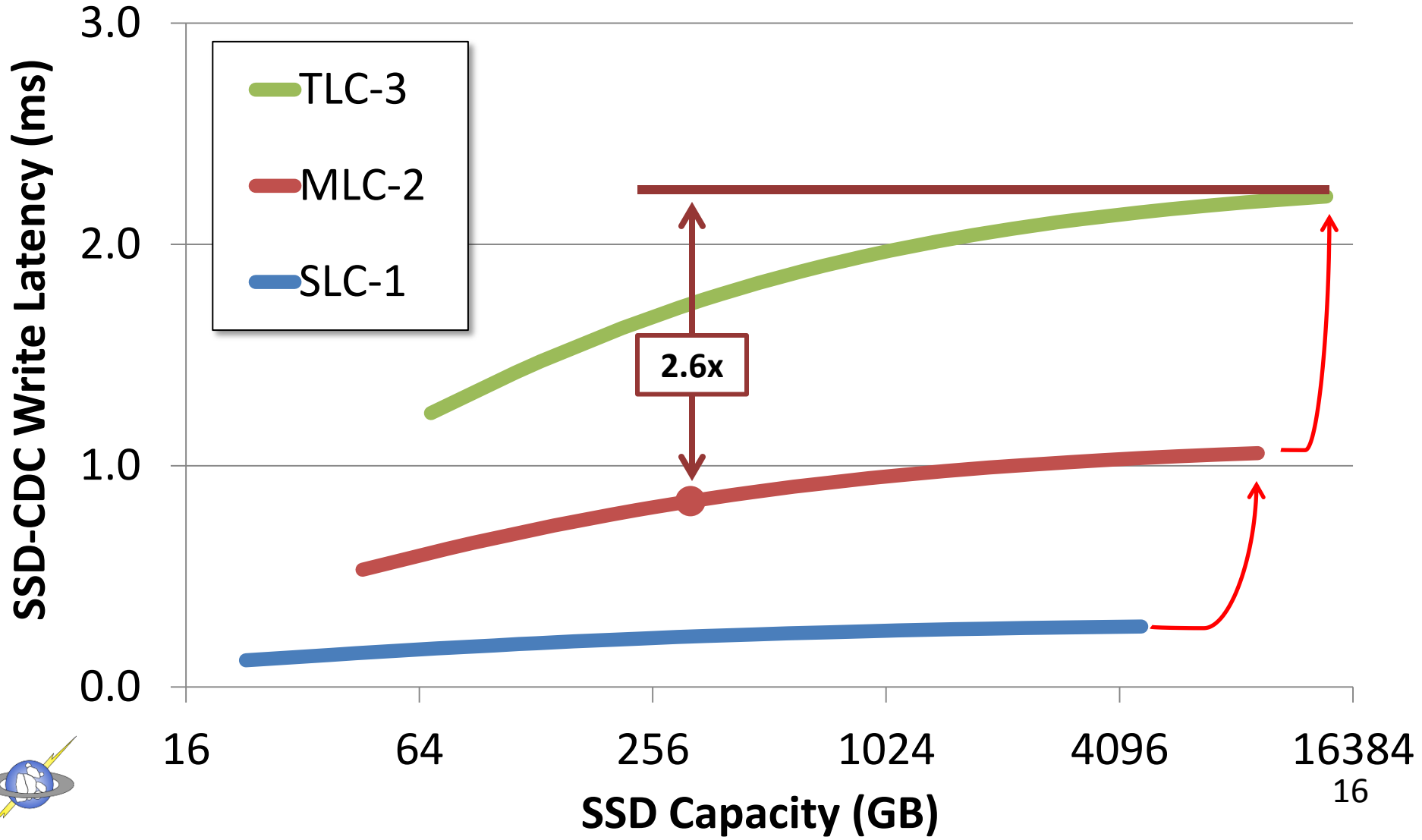
Empirical Data



Scaling Trends in Empirical Data



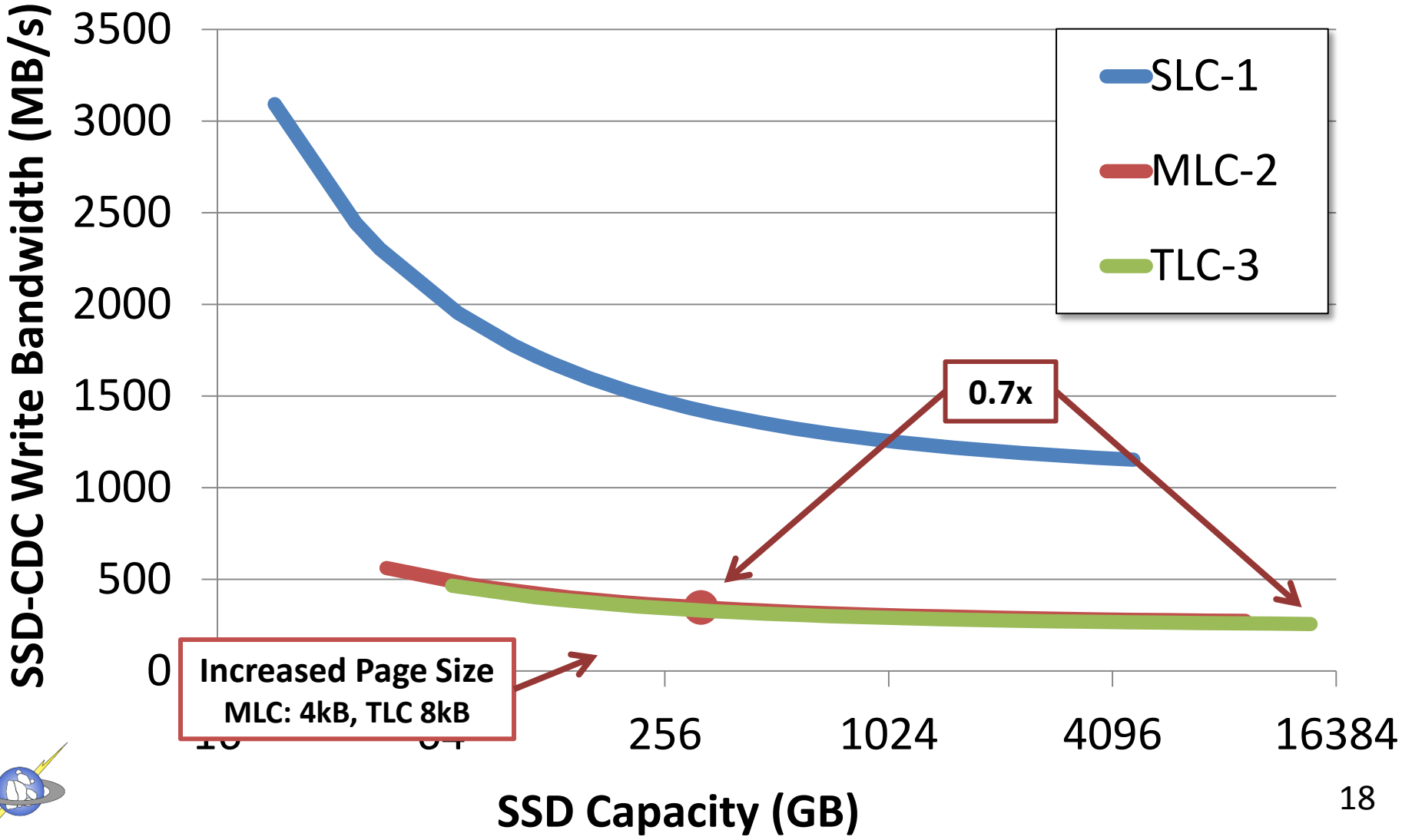
Write Latency of SSD-CDC



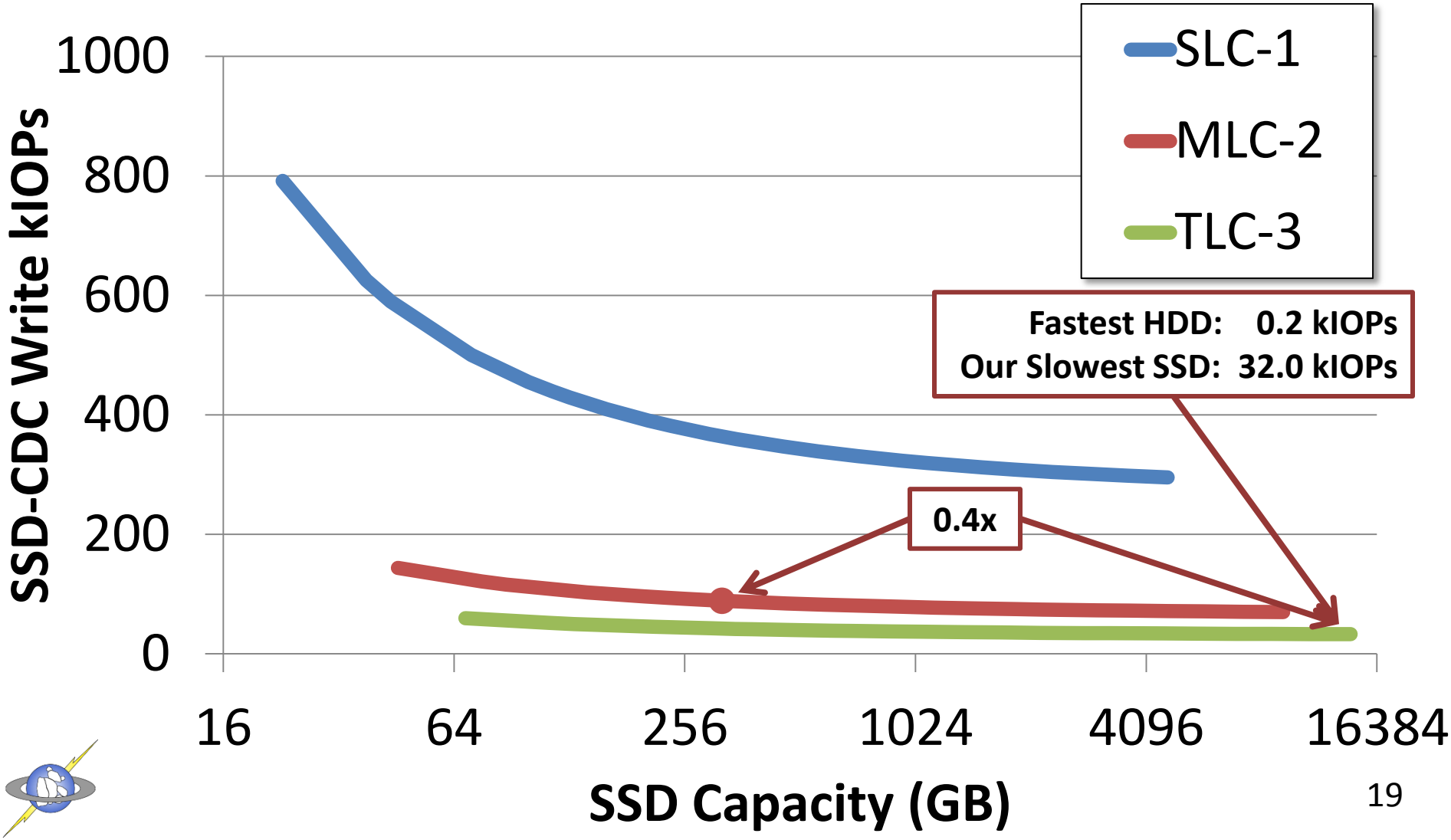
The Metrics

- Capacity: 43x
- Latency: 2.6x
- Throughput

Reduced Bandwidth

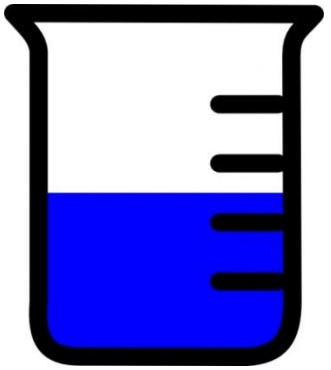


IOPs – 512B Random Accesses



The Metrics

- Capacity: 43x



- Latency: 2.6x

- Throughput: 0.7x, 0.4x

Conclusion

- Chip Scaling: A Mixed Bag
  - Improved: Density and Cost
  - In Decline: Performance and Reliability
- SSDs: Not always a perfect replacement for disks
  - Do Get: High Capacity & High IOPs
  - Don't Get: Low Cost & Low Latency

Questions?

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Non-volatile Systems Laboratory

Microsoft®
Research

The Model's Equations

Metric	Equation
Capacity	$Capacity_{Baseline} \times \left(\frac{BitsPerCell_{projected}}{BitsPerCell_{baseline}}\right) \times \left(\frac{FeatureSize_{baseline}}{FeatureSize_{projected}}\right)^2$
Latency	$ChipLatency + OverheadLatency$
Bandwidth	$ChannelCount \times \left(\frac{(diesPerChannel - 1) \times PageSize}{ChipLatency}\right), Operation \gg Bus\ Speed$
IOPs	$ChannelCount \times \left(\frac{(diesPerChannel - 1)}{ChipLatency}\right), Operation \gg Bus\ Speed$

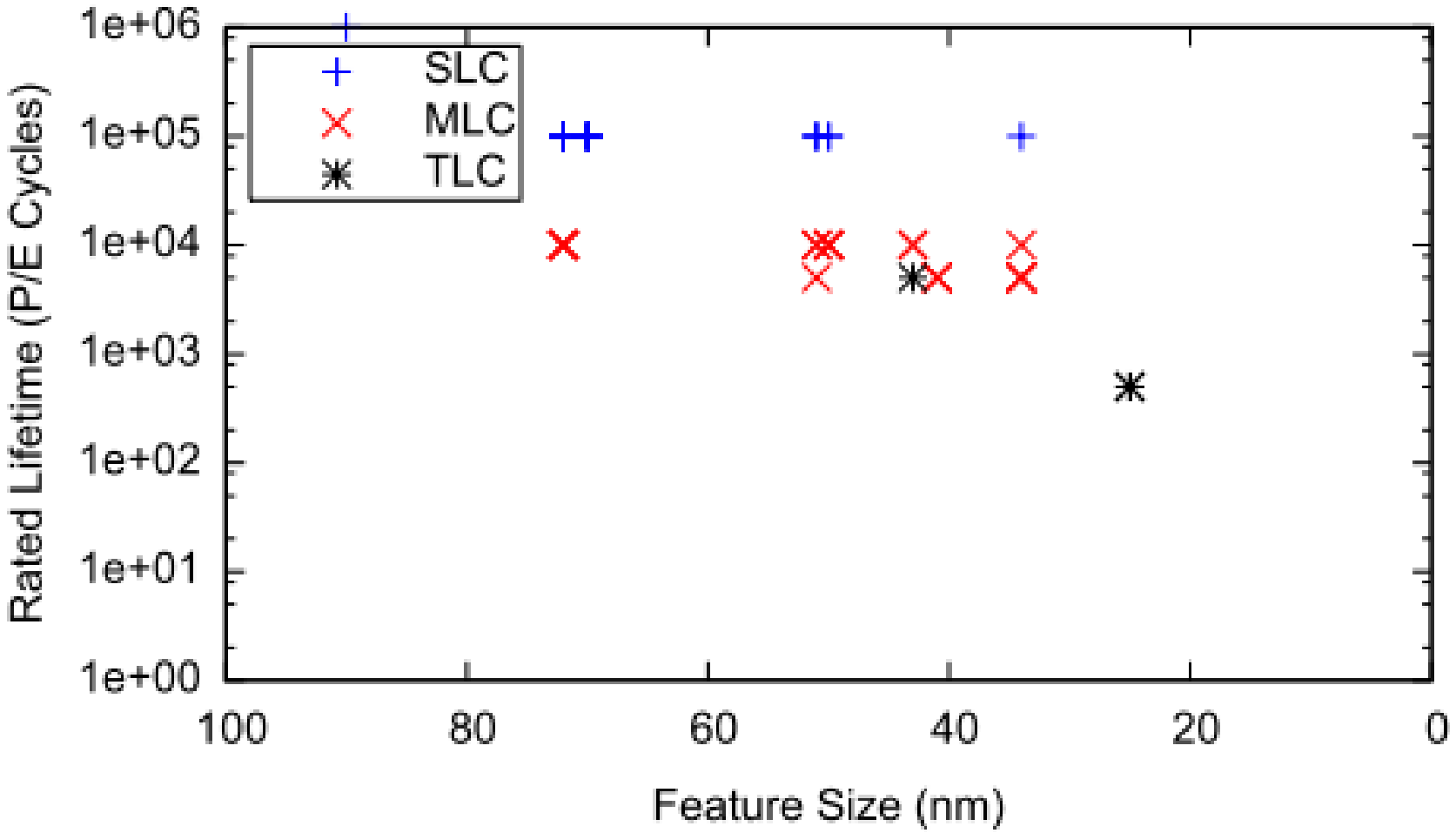
Measured Value

Baseline SSD Design

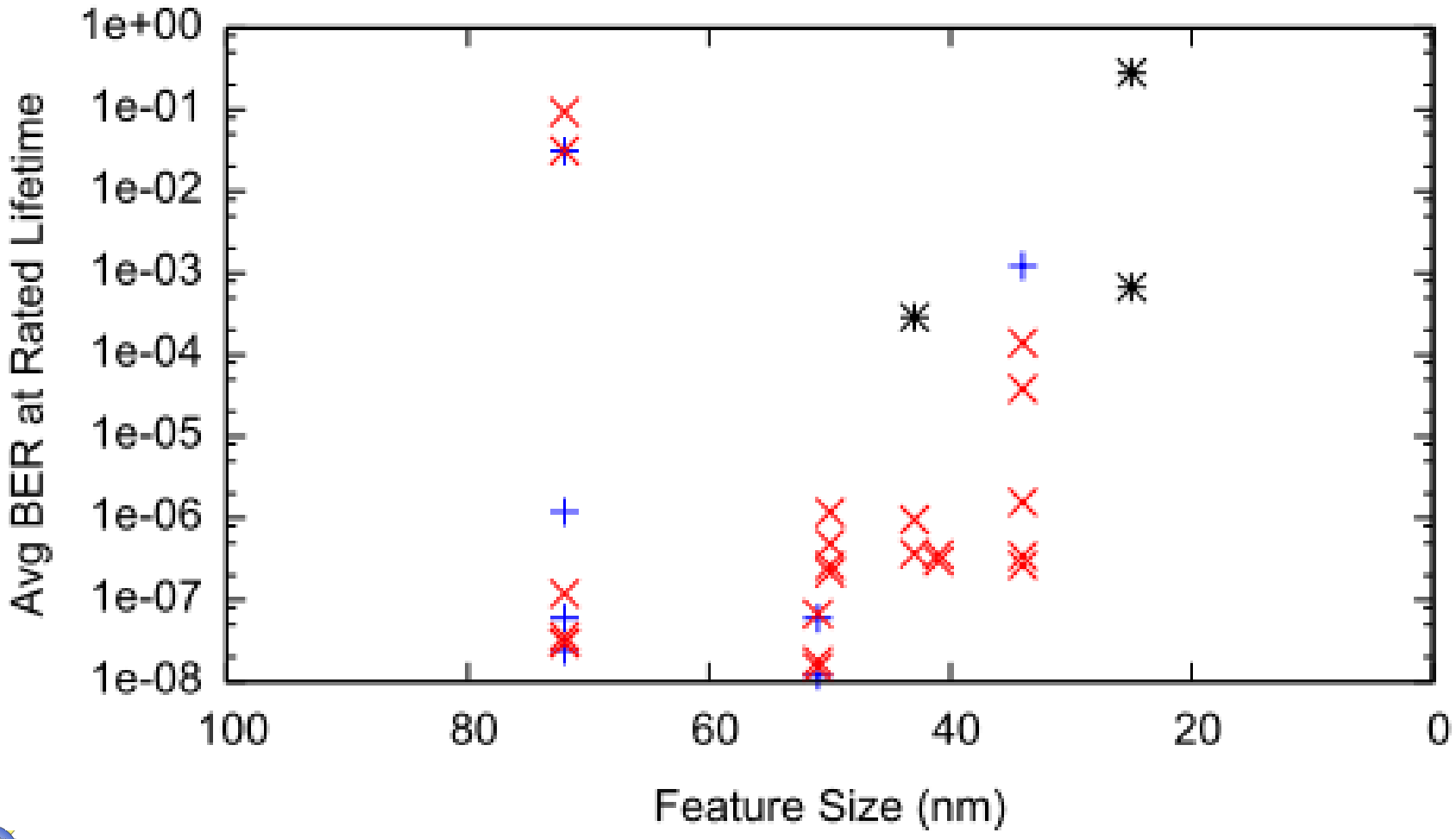
Projected SSD Design

Constant SSD Parameter

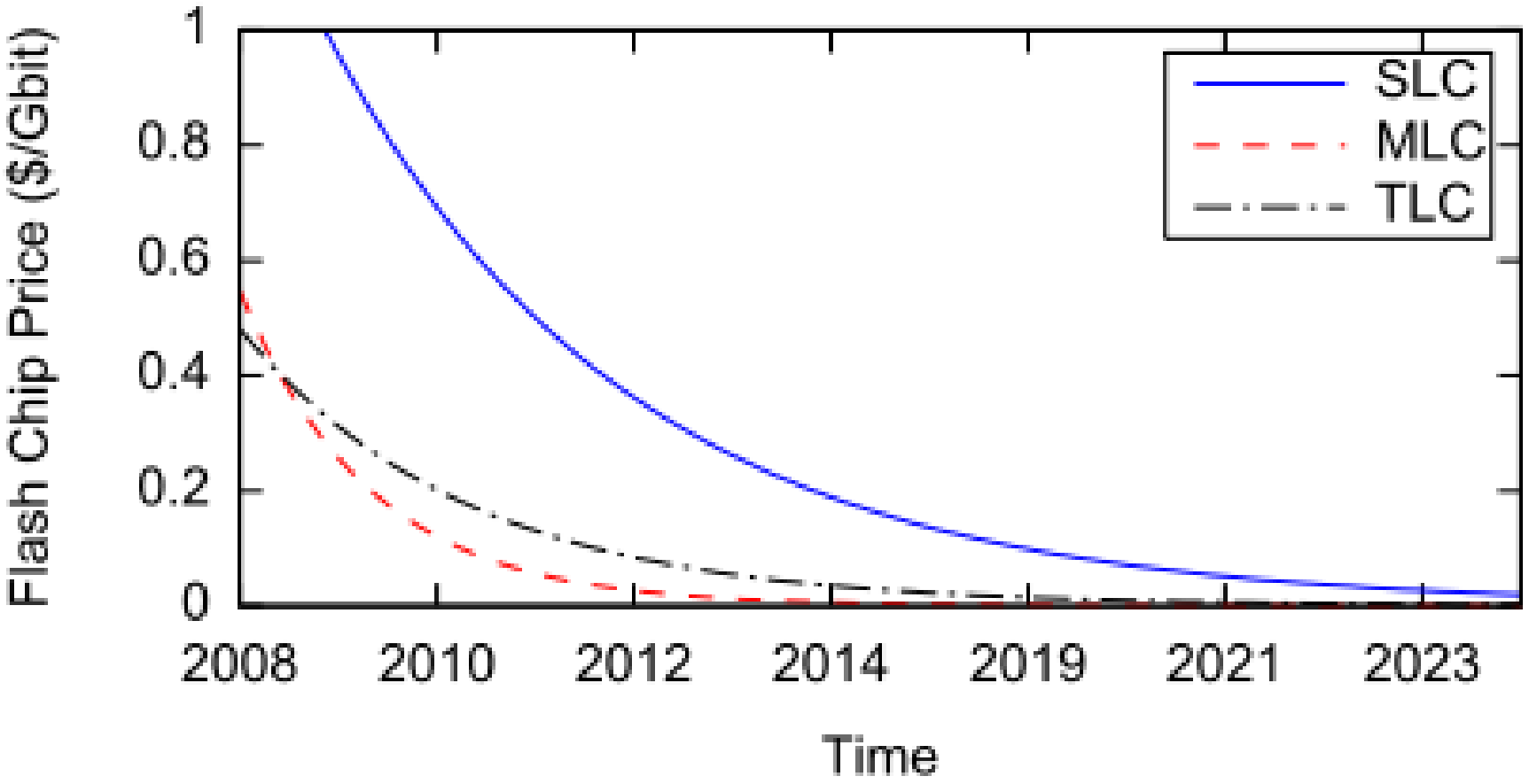
Lifetime


SLC
MLC
TLC
Rated Lifetime (P/E Cycles)
1e+06
1e+05
1e+04
1e+03
1e+02
1e+01
1e+00
100
80
60
40
20
0
Feature Size (nm)

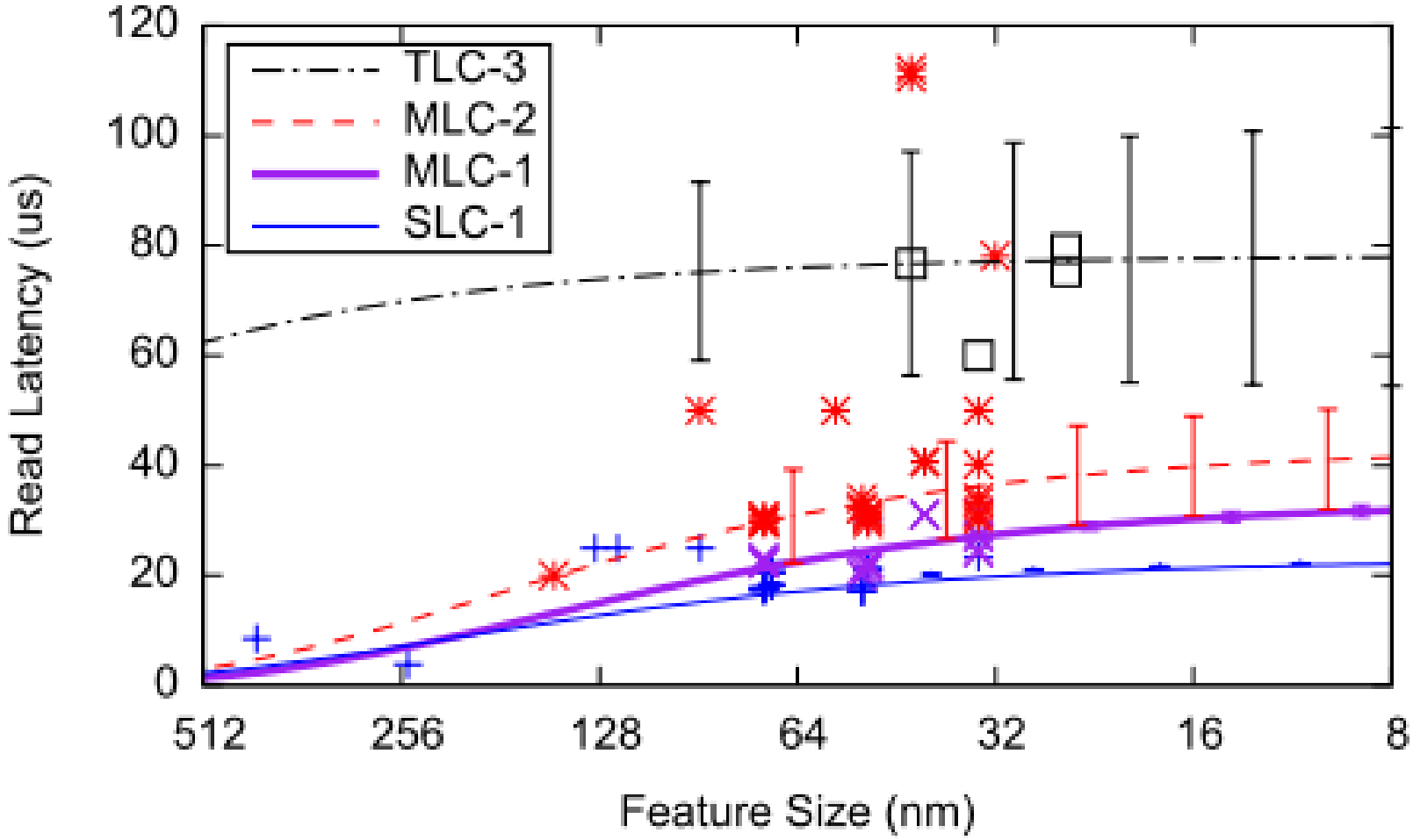
Error Rates


Avg BER at Rated Lifetime
1e+00
1e-01
1e-02
1e-03
1e-04
1e-05
1e-06
1e-07
1e-08
100
80
60
40
20
0
Feature Size (nm)

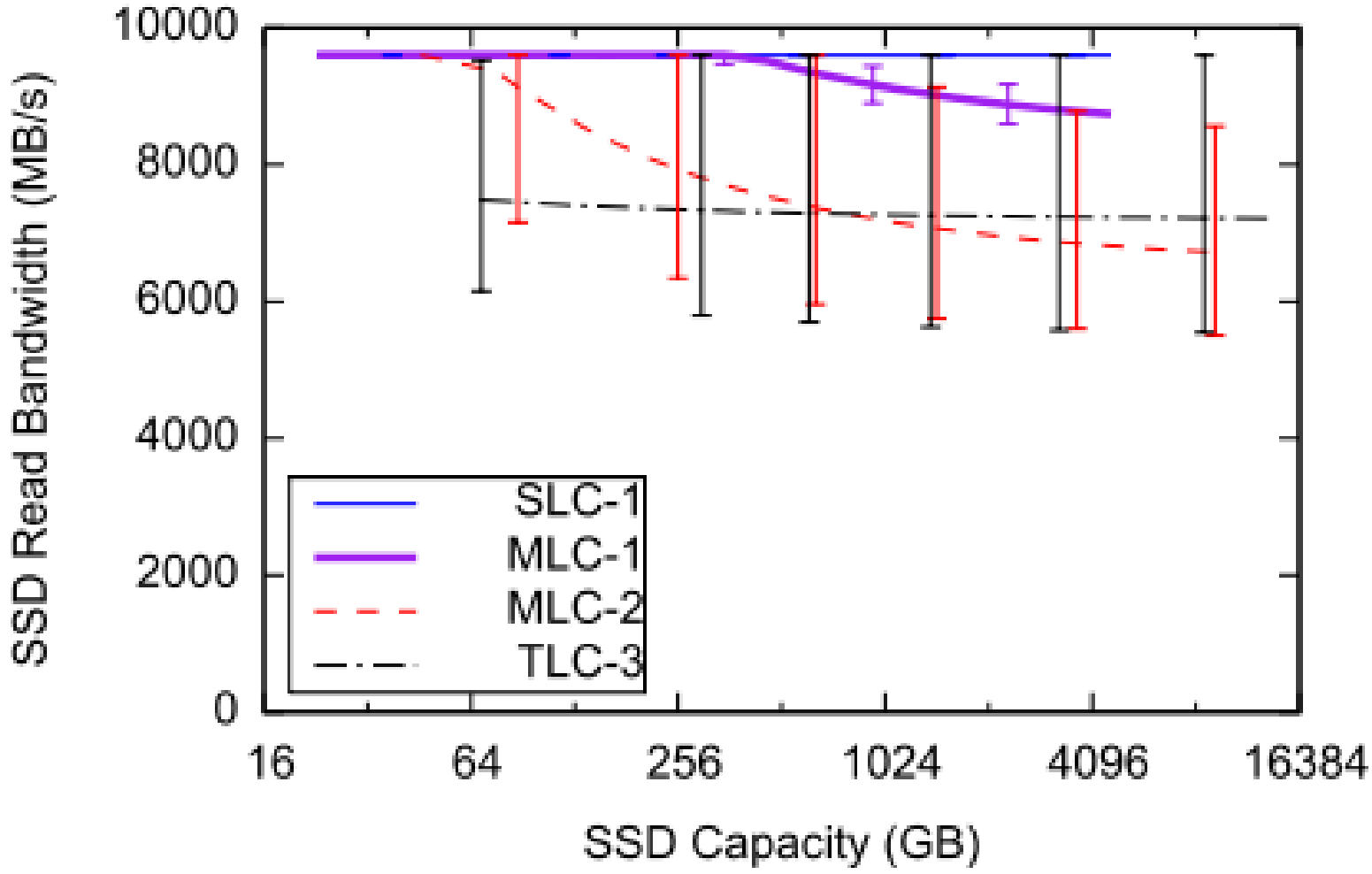
Price


Flash Chip Price ($/Gbit)
1
0.8
0.6
0.4
0.2
0
2008
2010
2012
2014
2019
2021
2023
Time
SLC
MLC
TLC

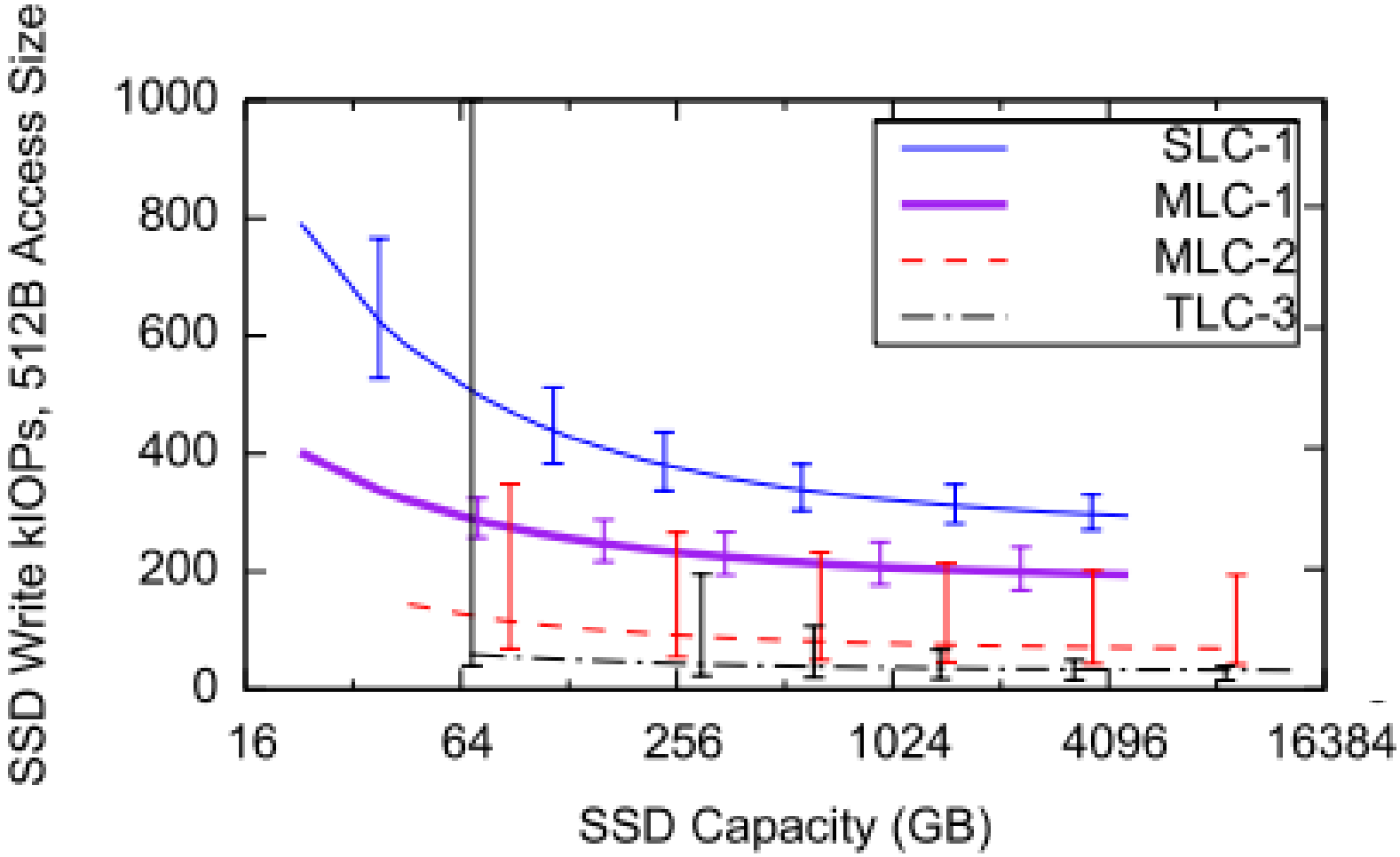
Read Latency



Read Bandwidth



Read IOPS – 512B Random Access



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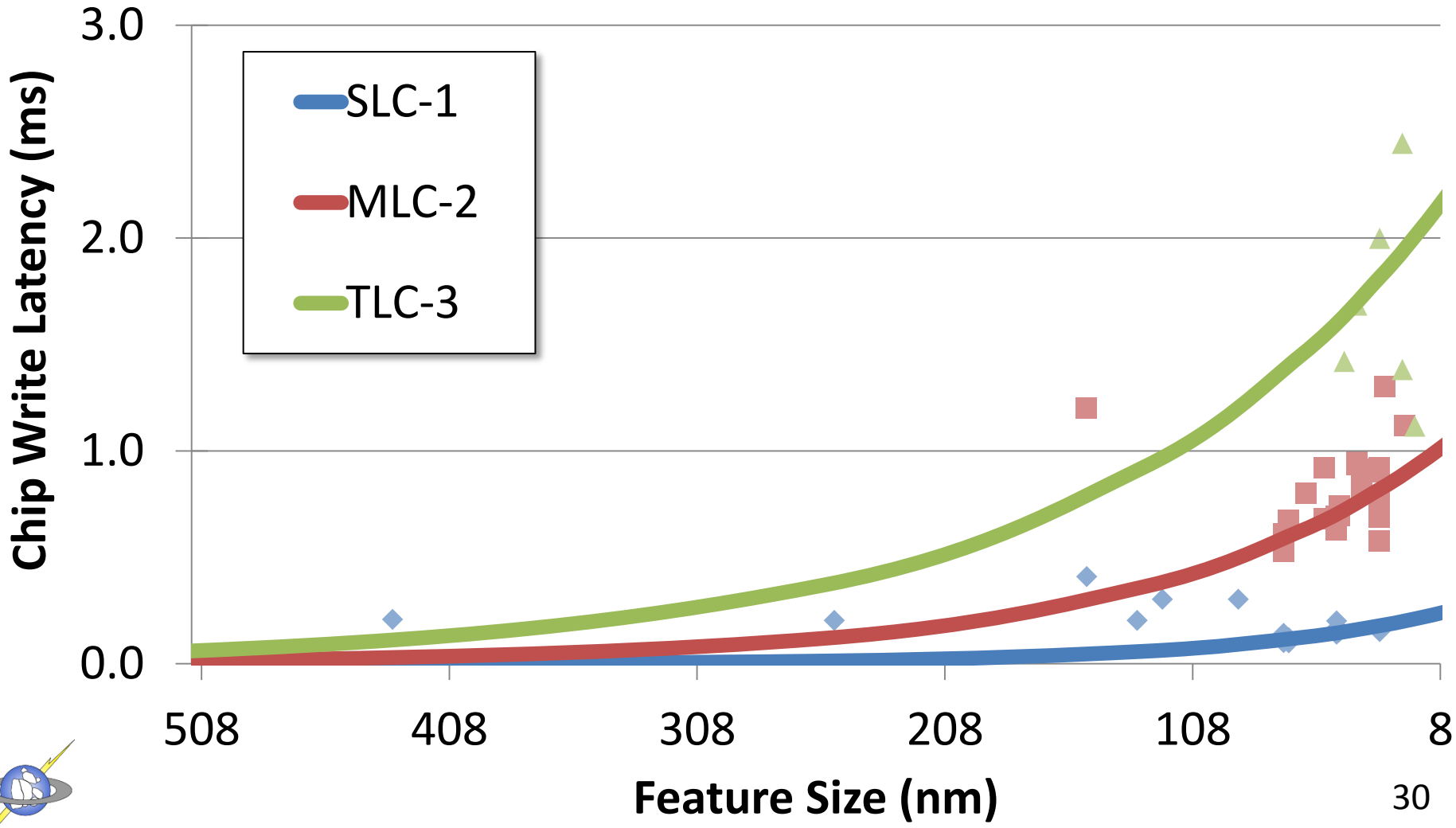

Increasing Density: Multi-bit Cells